Electrical Energy Conversion and Power Systems

Universidad de Oviedo

Power PCB Design

Components that produce EMI

Magnetic components

Oscillators, micro-controlers

High frequency switches

Mechanical elements
reley

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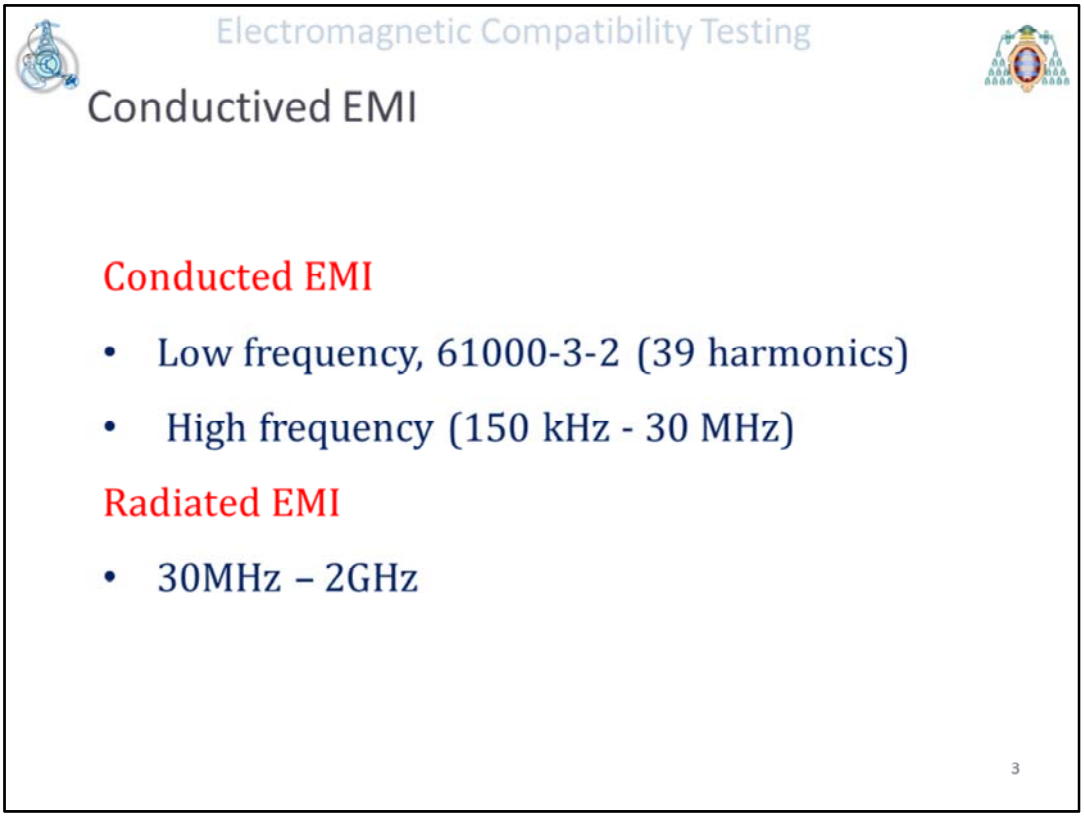
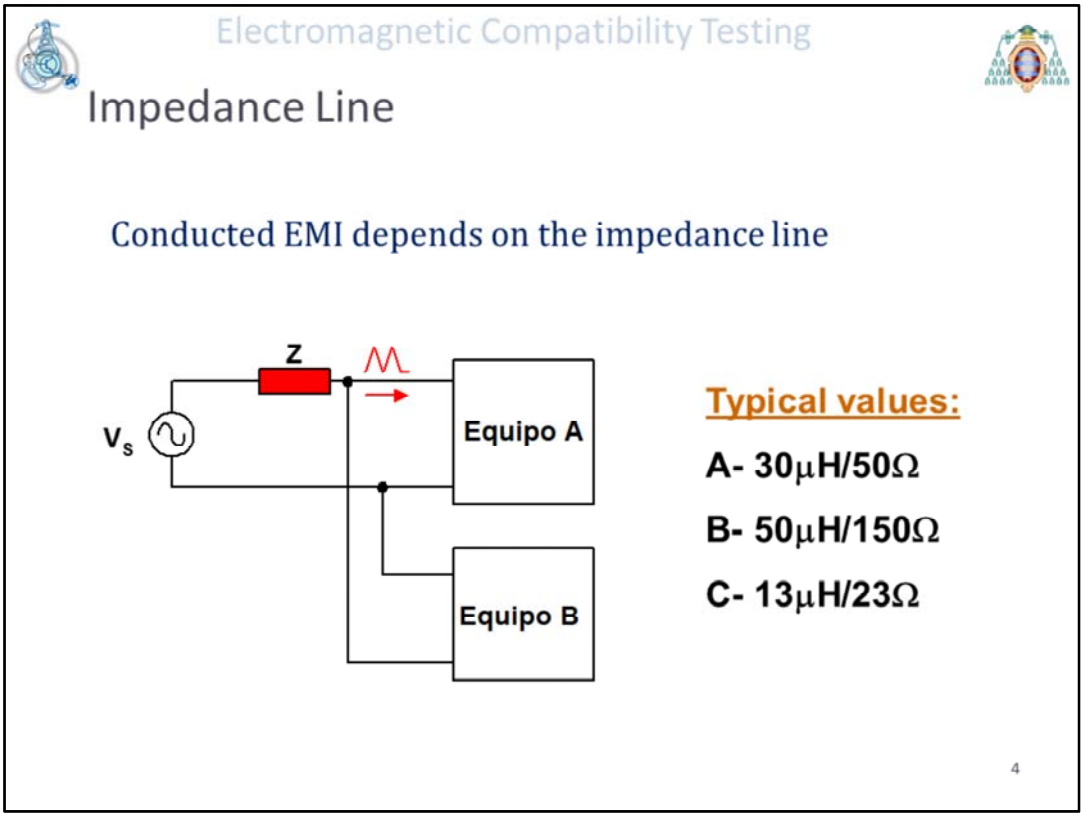
In electronic circuits we can identify several characteristic elements capable of generating electromagnetic noise



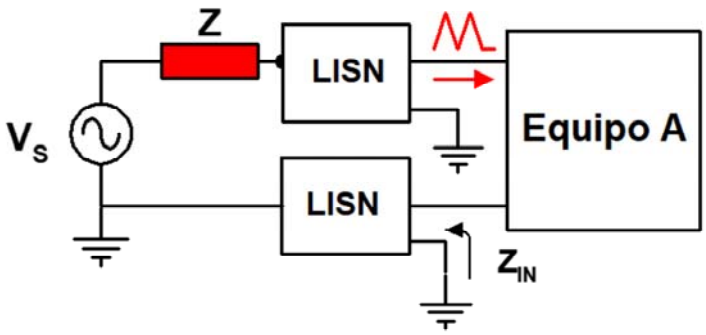
The frequency margins to be analyzed in the EMC regulations range from Hz to GHz



A key element for measuring the noise conducted is the LISN. This equipment allows guaranteeing a 50-ohm line impedance for the entire frequency range considered in this test (150kHz-30MHz)

LISN (Line Impedance Stabilizing Network)

$Z_{IN}=50\Omega$



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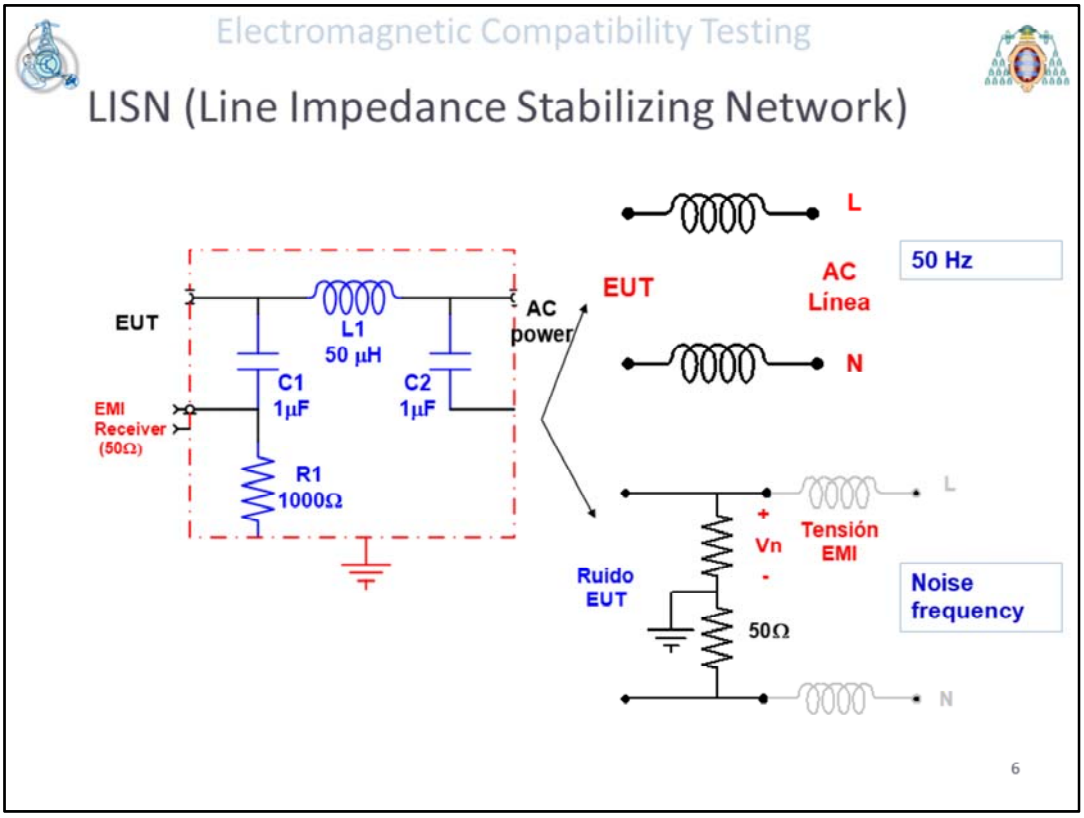
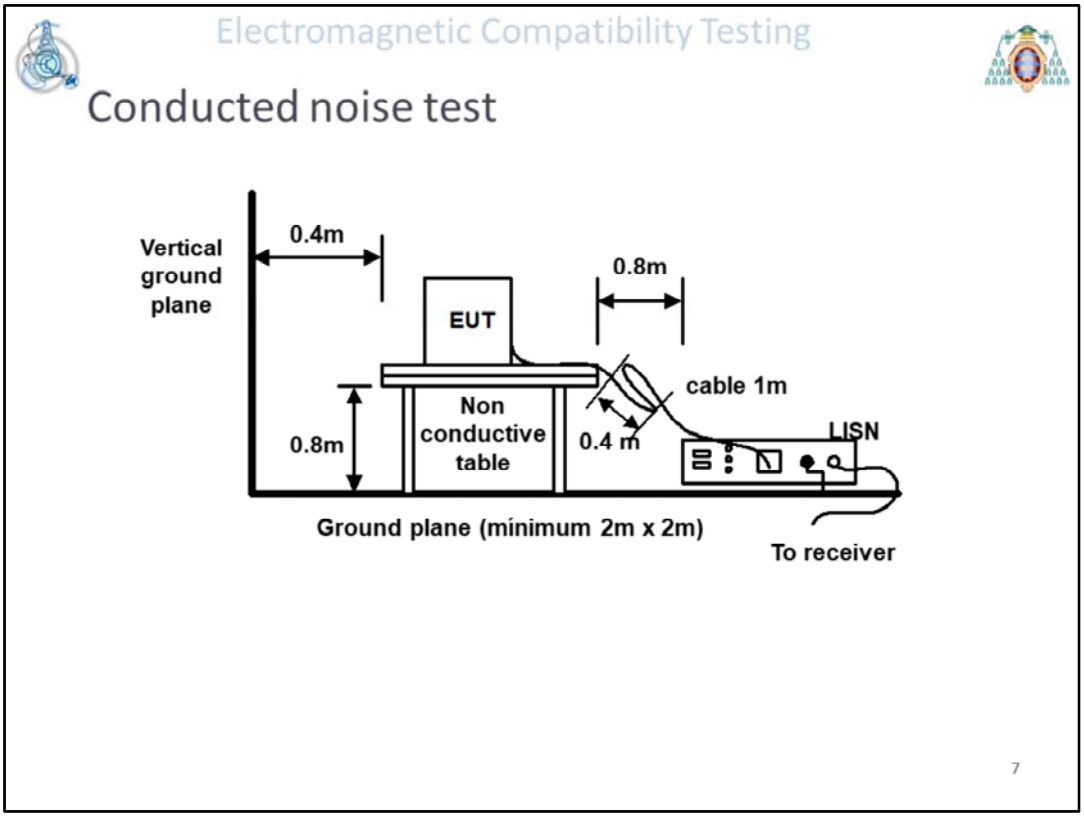
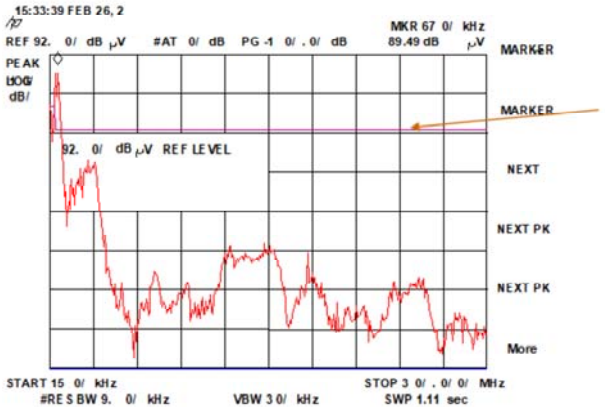


The basic internal scheme of the LISN can be split into two models depending on the frequency considered: 50Hz or high frequency



The drawing shows the distribution of the equipment during the conducted emission test. The position of the cables must be pointed out: this may seem unimportant but it causes that the measures may vary when performed by several laboratories.

Conducted Disturbances



Limit

Bandwidth:

10 kHz-150 KHz, RBW=200 Hz
150 kHz-30 MHz, RBW=9 kHz

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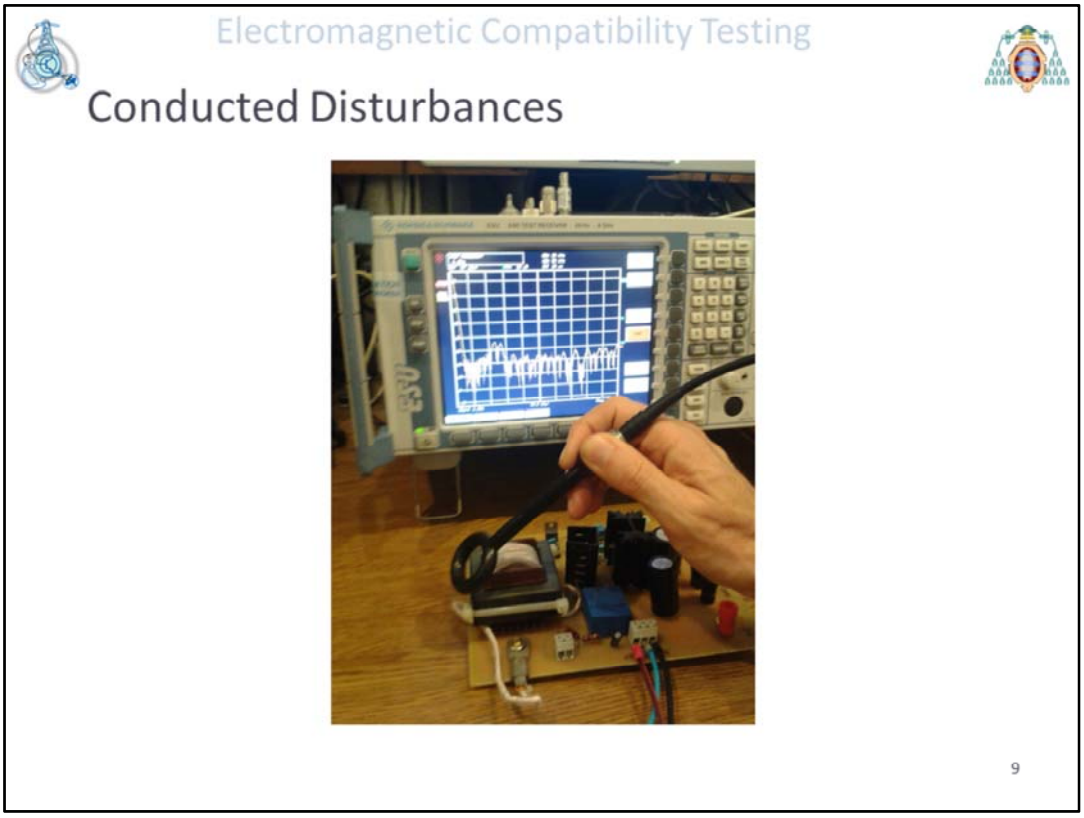
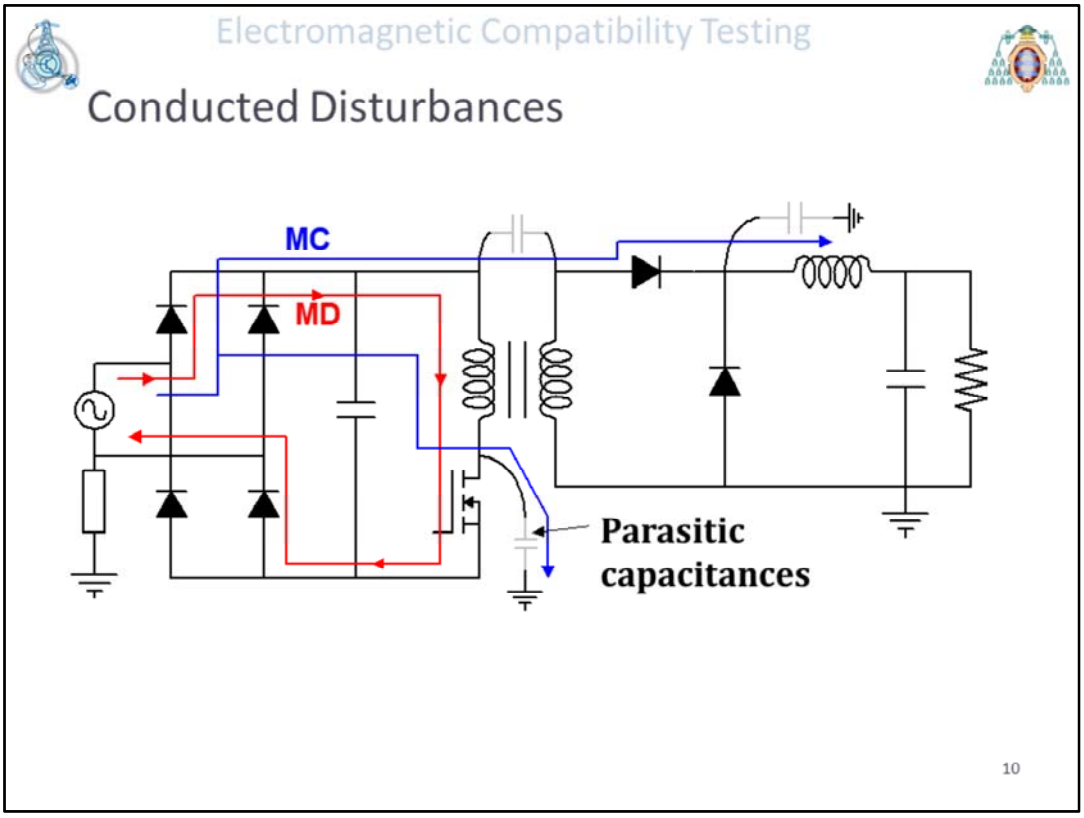
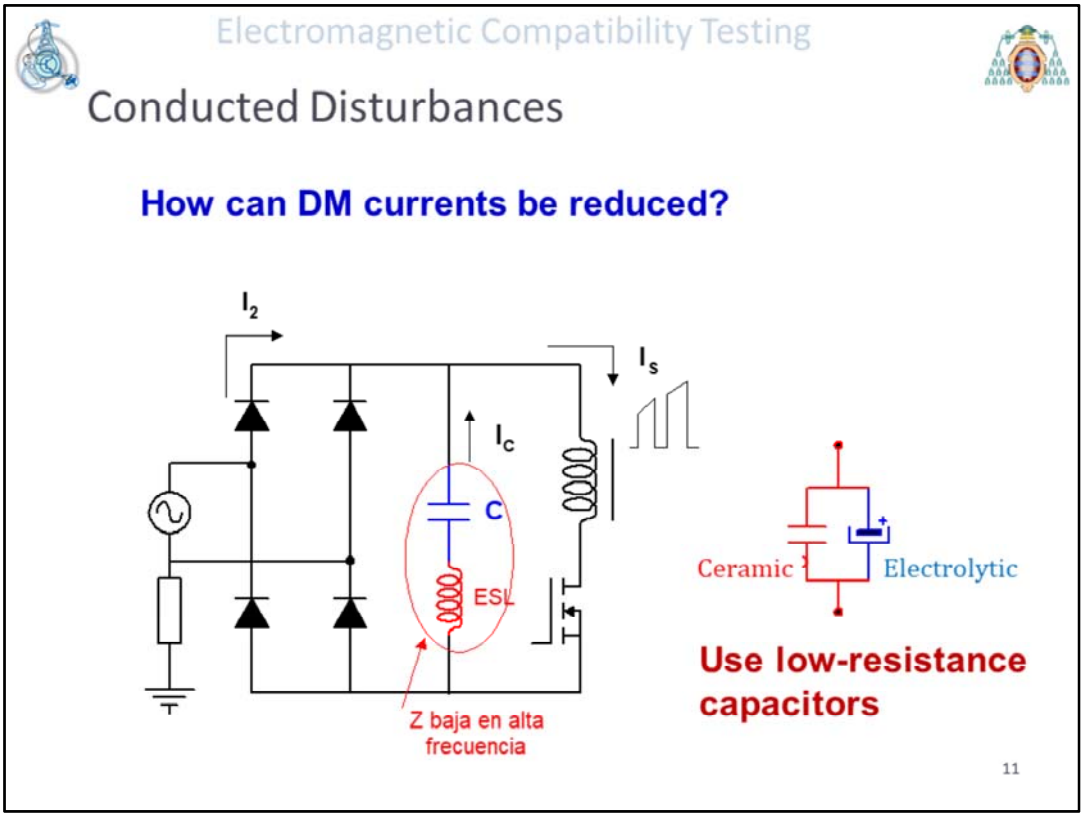
Another parameter to take into account is the resolution bandwidth (RBW). This parameter is defined for each frequency range considered.



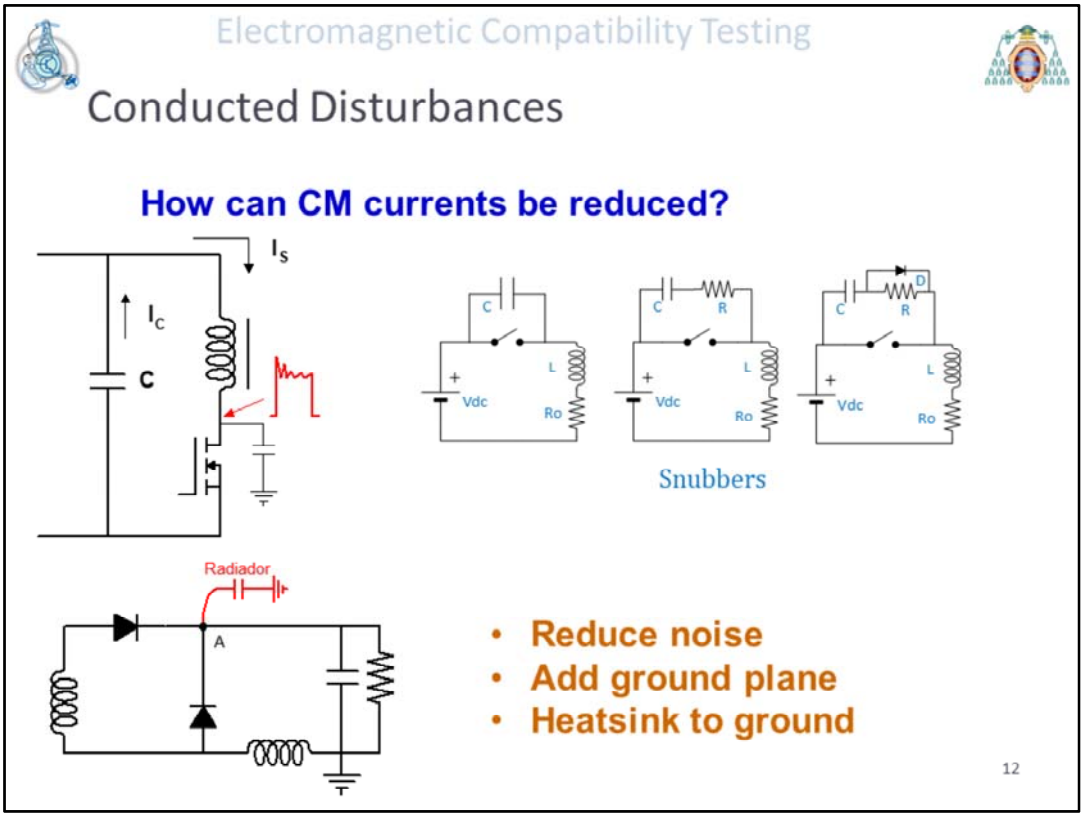
Field probes (electric, magnetic) can help to identify the noisy components in a system, but they do not allow knowing whether the equipment is going to pass the test.



In electronic systems we can identify currents in differential mode (DM), responsible for transferring the energy to the load, and common-mode (CM) currents, which flow through parasitic capacitances and return through the mass of the circuit.

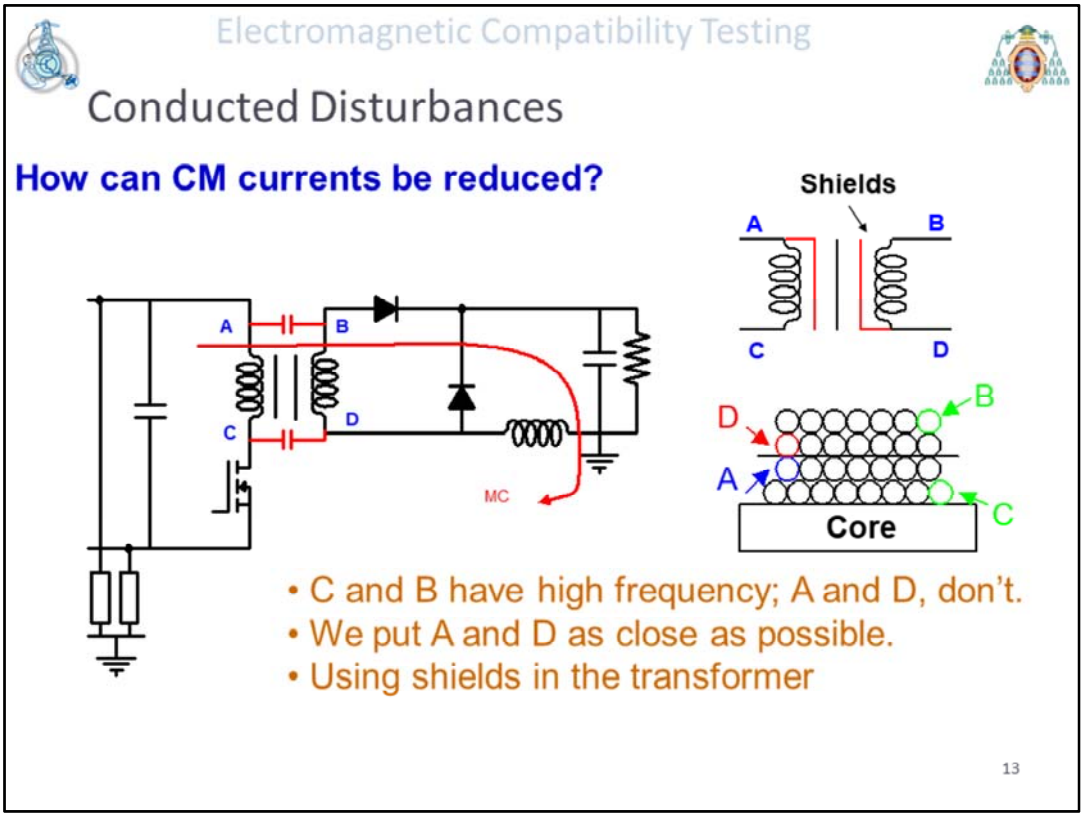


When we want to reduce the high frequency harmonics present in the differential mode currents, we will incorporate filter capacitors capable of working properly at high frequency. Make sure that the capacitor connection is made with the lowest possible parasitic inductance.

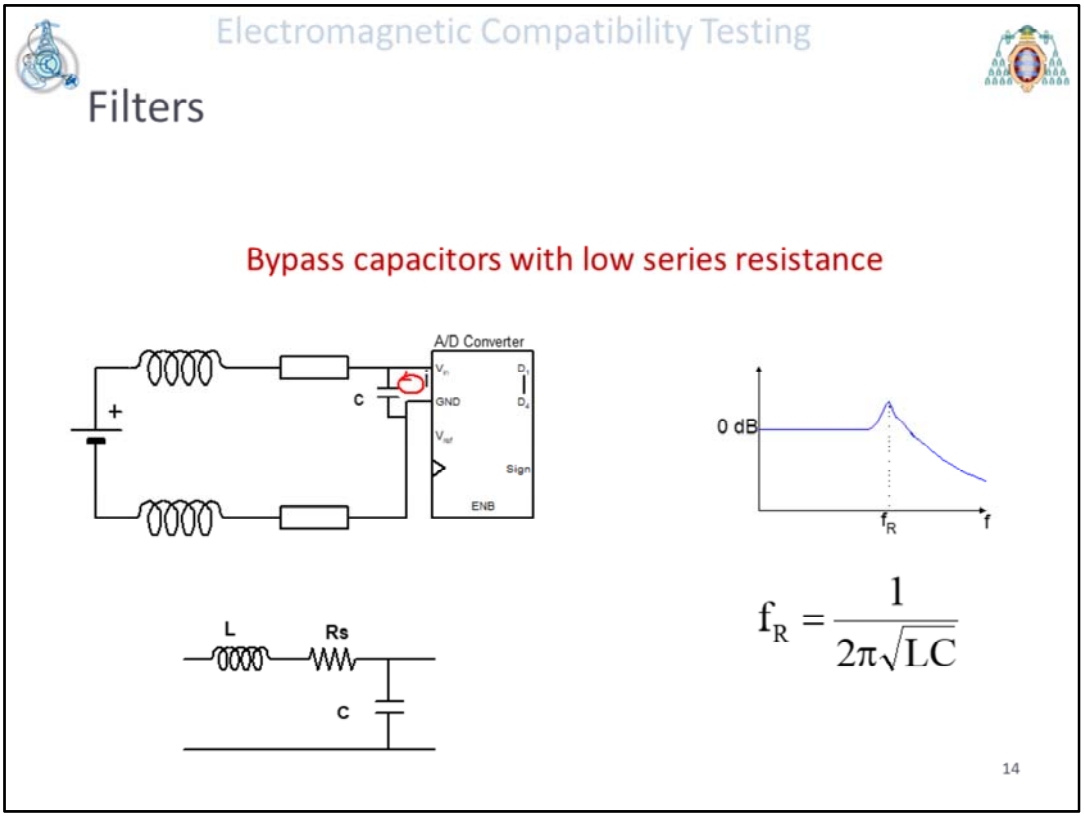


Not only does the incorporation of snubbers in the switches significantly reduce the emission of conducted noise, but it also has a very important effect in the reduction of radiated noise.

The switching of the transistors causes high-frequency harmonics that can find low-impedance path through the parasitic capacitances present in the circuit.



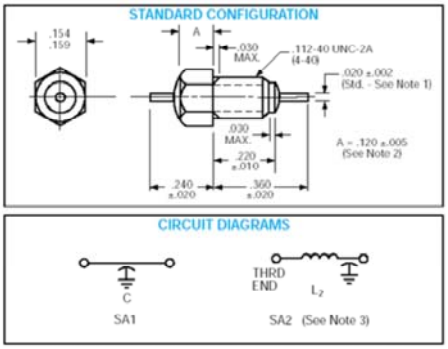
Some transformer manufacturing techniques help us to reduce the parasitic capacities present between windings. In order for this to be done, noisy terminals (terminals where there is a greater variation of voltage) must be moved away from each other. By doing so, the parasitic capacity between windings will be reduced and common-mode currents will find a path of greater impedance.

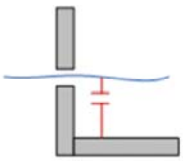


The use of bypass capacitors is another of the most common techniques for filtering the power lines of integrated circuits. These capacitors do not require high capacities but a good behavior in high frequency.

Filters (from AVX catalogue)

Bolt style EMI filter (10 MHz-26 GHz)

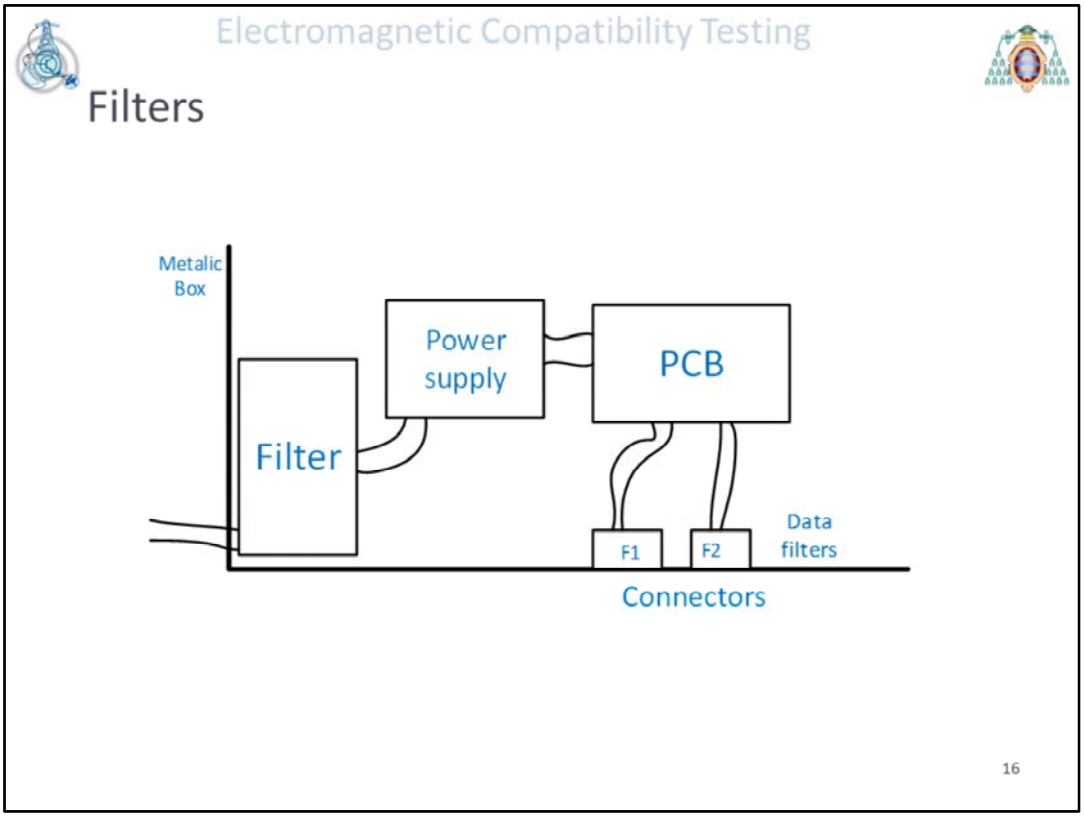




SPECIFICATIONS

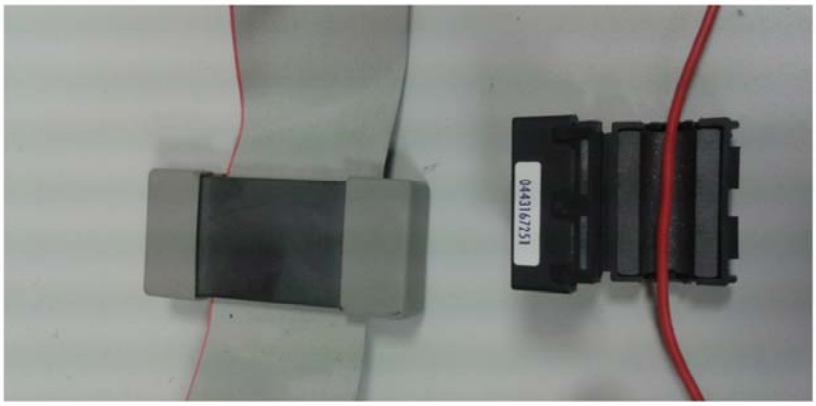
					Insertion Loss² Per MIL-STD-220, +25°C					
AVX P/N	CKT	CAP¹	DC Voltage	DCR	1 MHz	10 MHz	100 MHz	200 MHz	1 GHz	10 GHz
SA1C1-102	C	1000	50	.02	–	4	20	25	25	55
SA1C1-502	C	5000	50	.02	–	15	34	41	42	55
SA1C1-103	C	.01	50	.02	4	21	35	42	50	70
SA1C1-273	C	.027	50	.02	10	30	39	43	65	70
SA1C1-503	C	.05	50	.02	15	35	42	45	70	70

There are commercial devices that allow a capacitor to be placed between the conductor terminal and the housing in which the circuit is located. These components reduce the noise that may come out of the shielding



Filters are normally placed in the inlets to guarantee a voltage supply clean of noise

Filters



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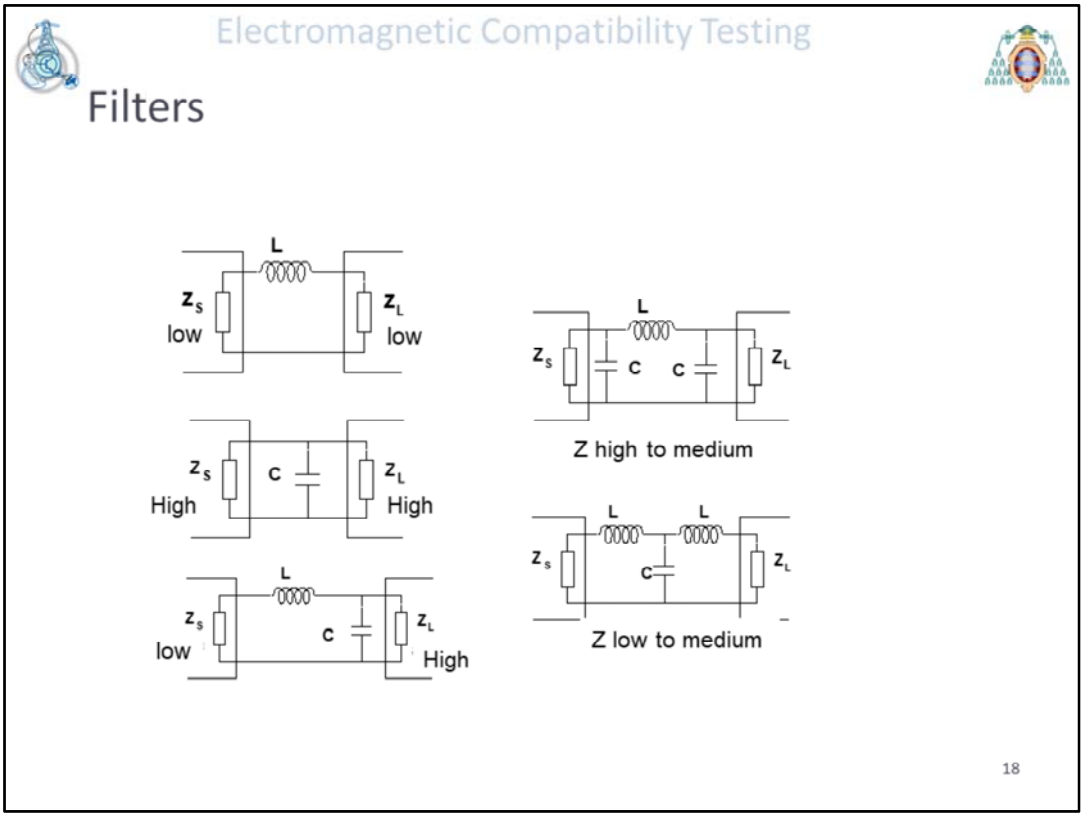
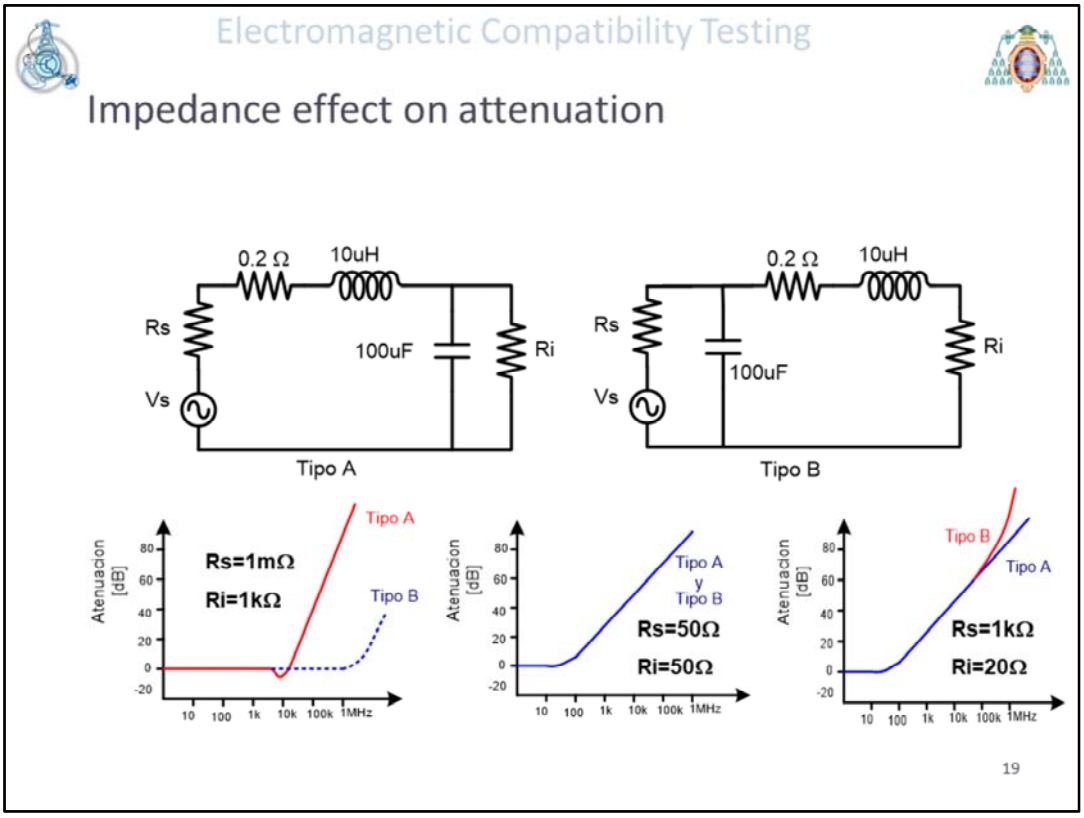
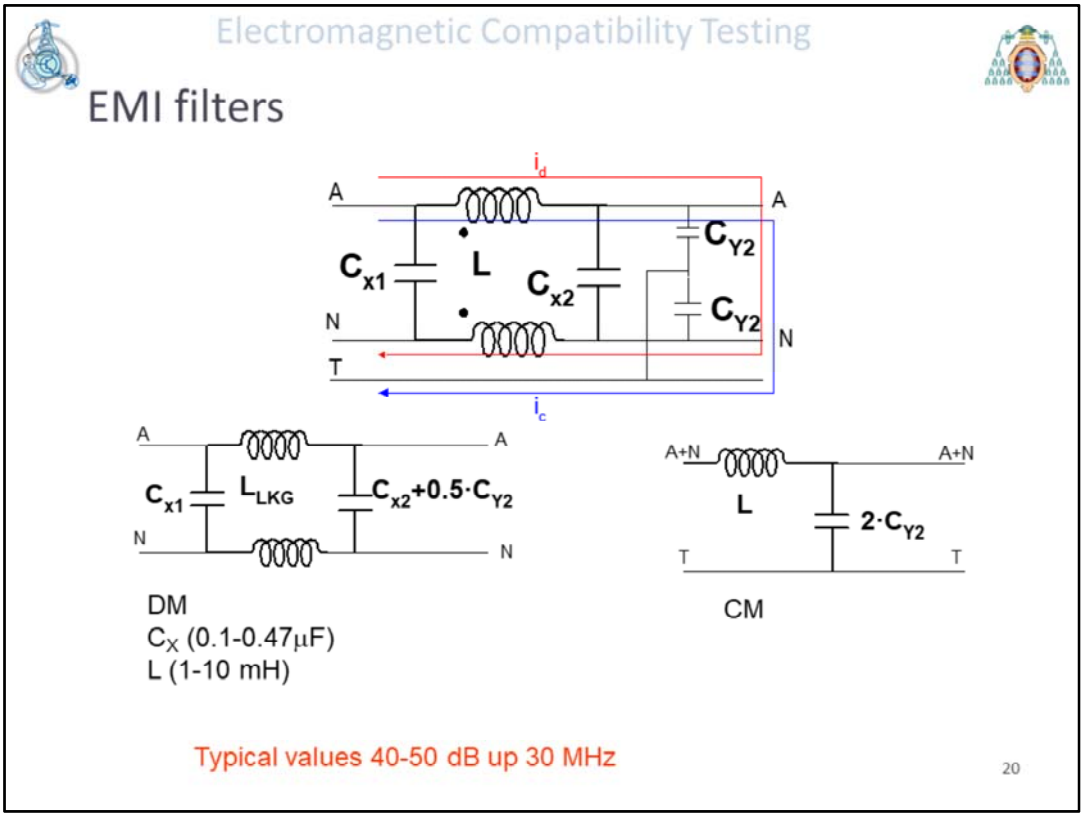
When it comes to filtering cables, there are several ferrite geometries that can be used



The selection of the filter type depends on the input and output impedance of the circuits that are interconnected. The figure shows various alternatives



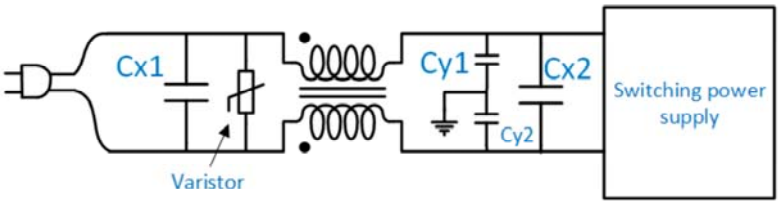
The plots show the attenuation achieved depending on the position of the capacitor and the coil.



When an AC source is used, an AC filter is usually incorporated at the input. These filters are designed to reduce common-mode currents with the magnetizing inductance of the coupled coils and capacitors C_Y. High-frequency harmonics in differential mode are filtered by the leakage inductance and the C_X capacitors fundamentally.

Use of a common-mode choke

Catalogue image



Reducing noise in line

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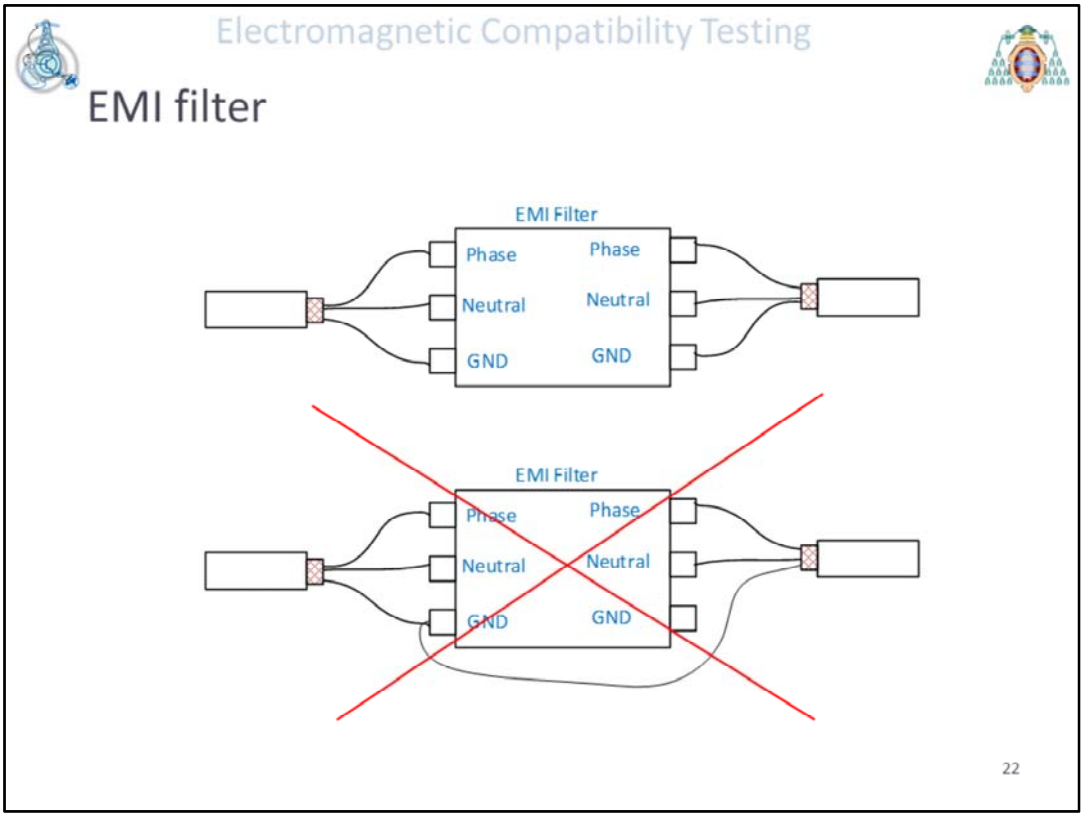
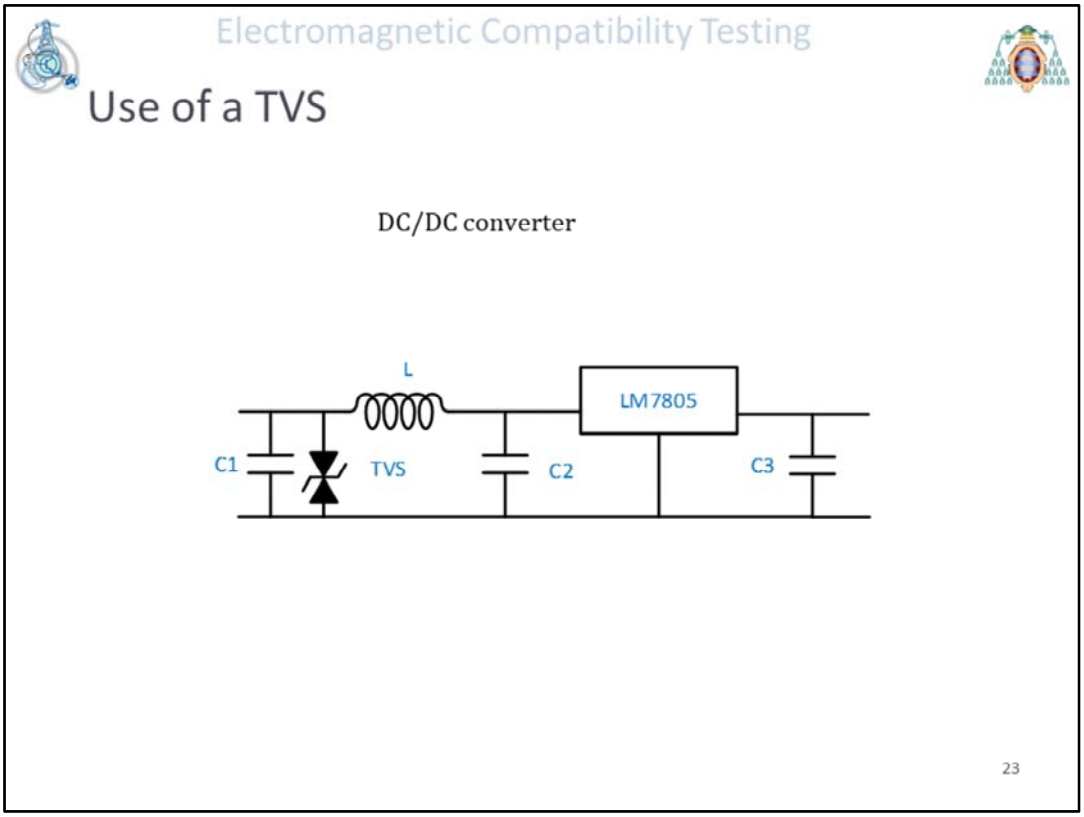
Arrangement of an AC filter



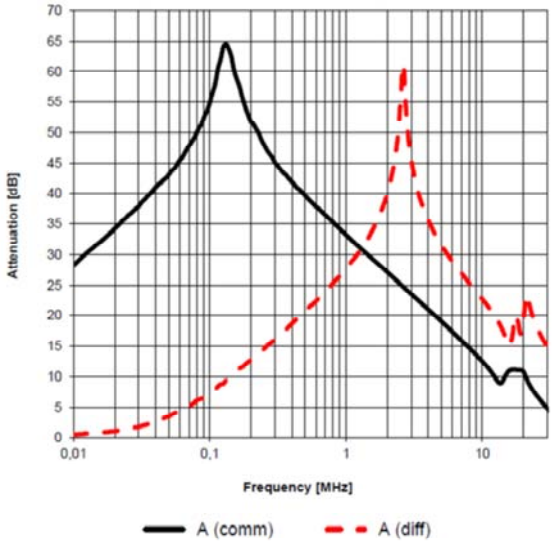
The ground terminal must not be connected outside the AC filter

Use of a TVS



A TVS can also be incorporated at the input of the power supplies

Use of a common-mode choke



WÜRTH ELEKTRONIK

Attenuation of the WE-CMB XS 39 mH

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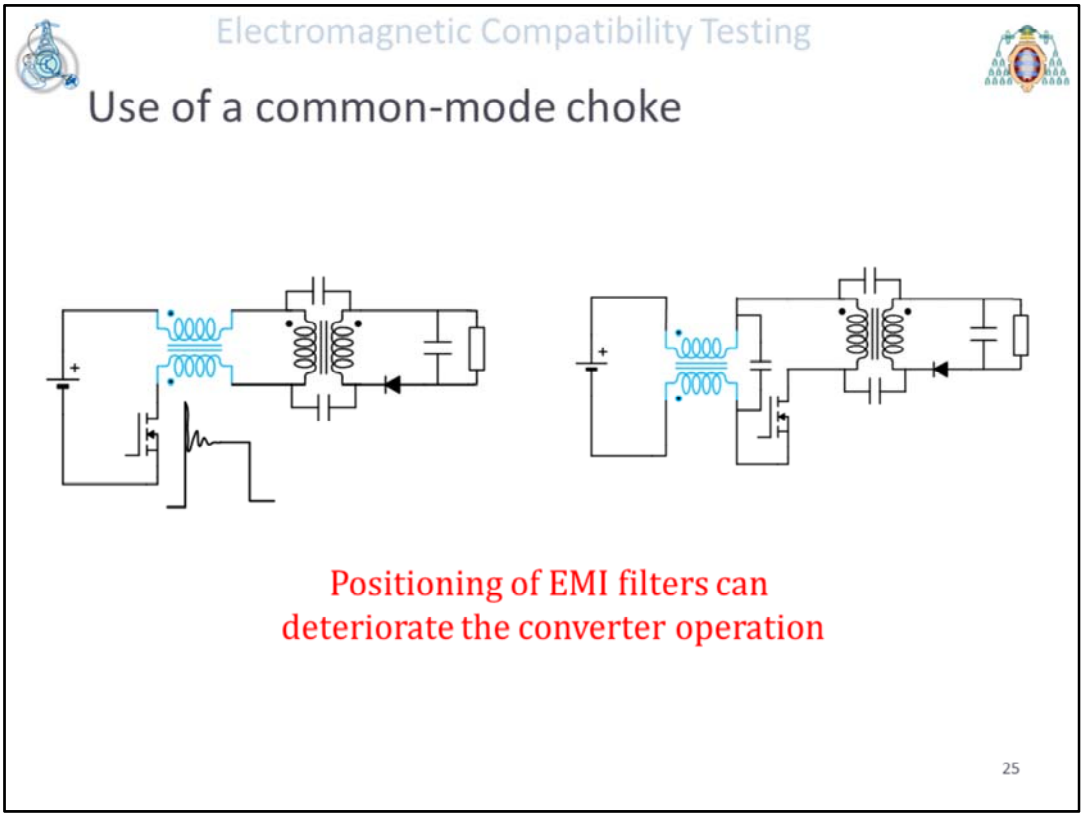
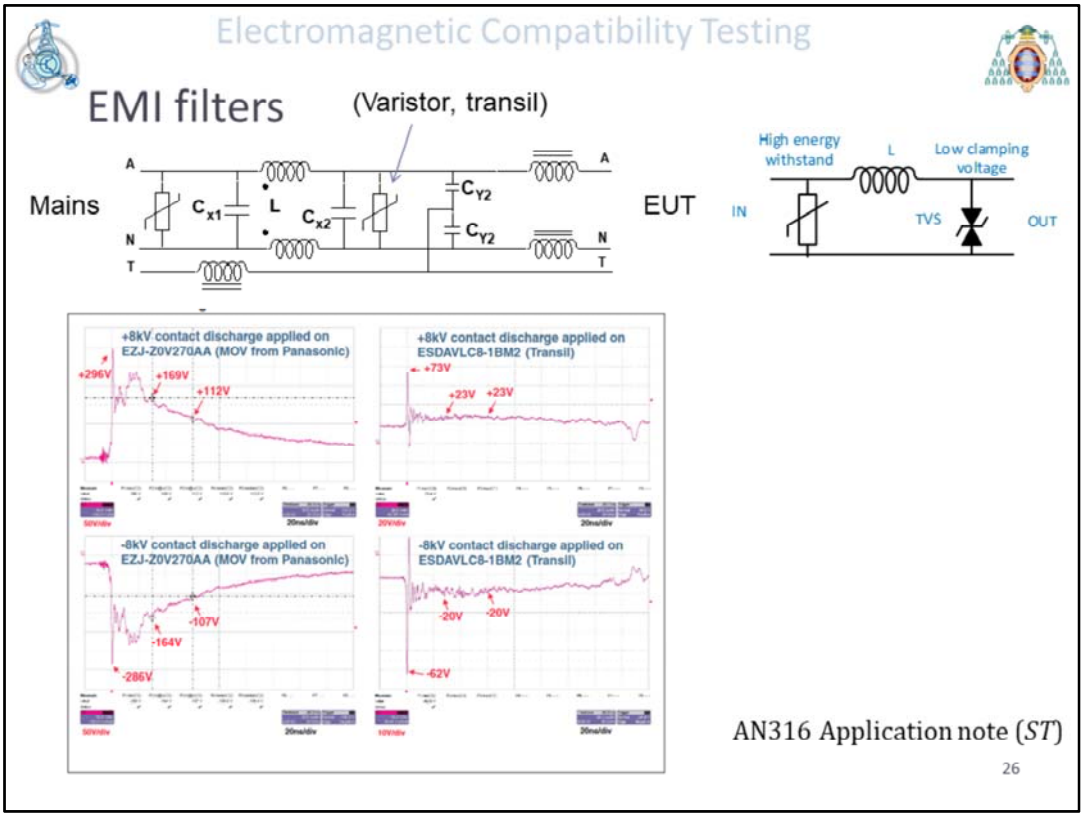
Attenuation curves for filter WE-CMB XS 39 from Wurth Elektronik (commercial catalogue)

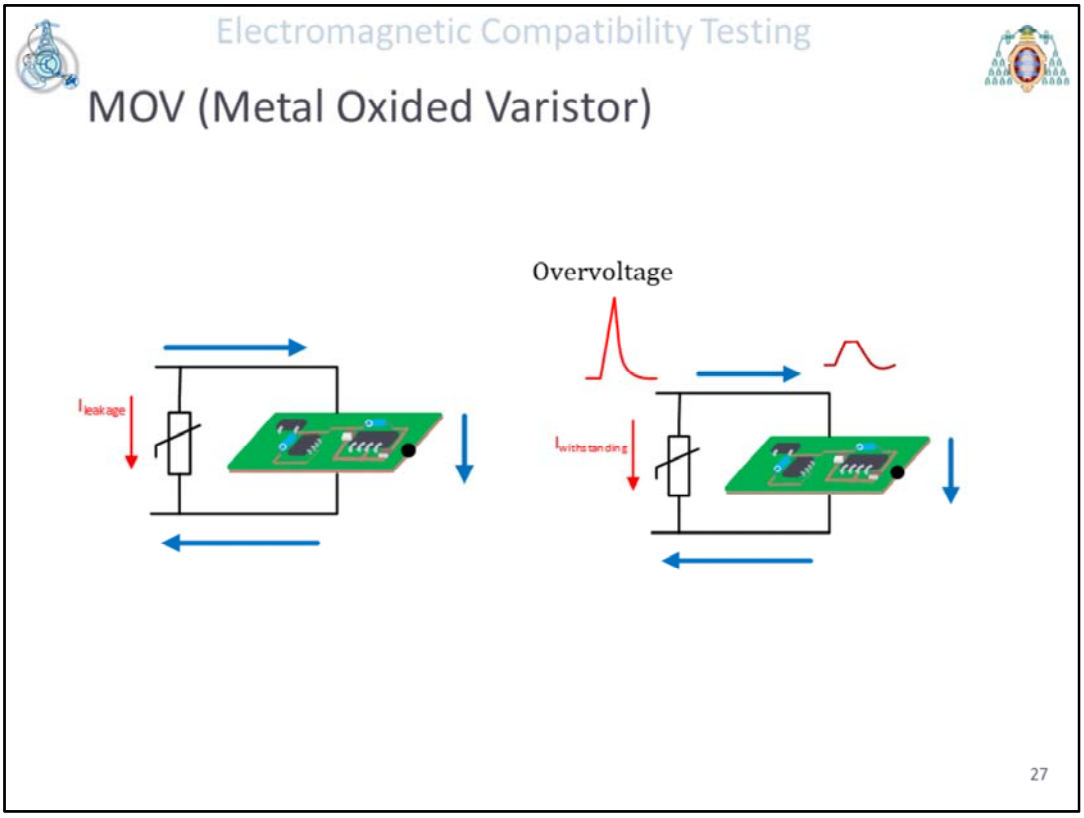


Special care must be taken with the positioning of the EMI filters.

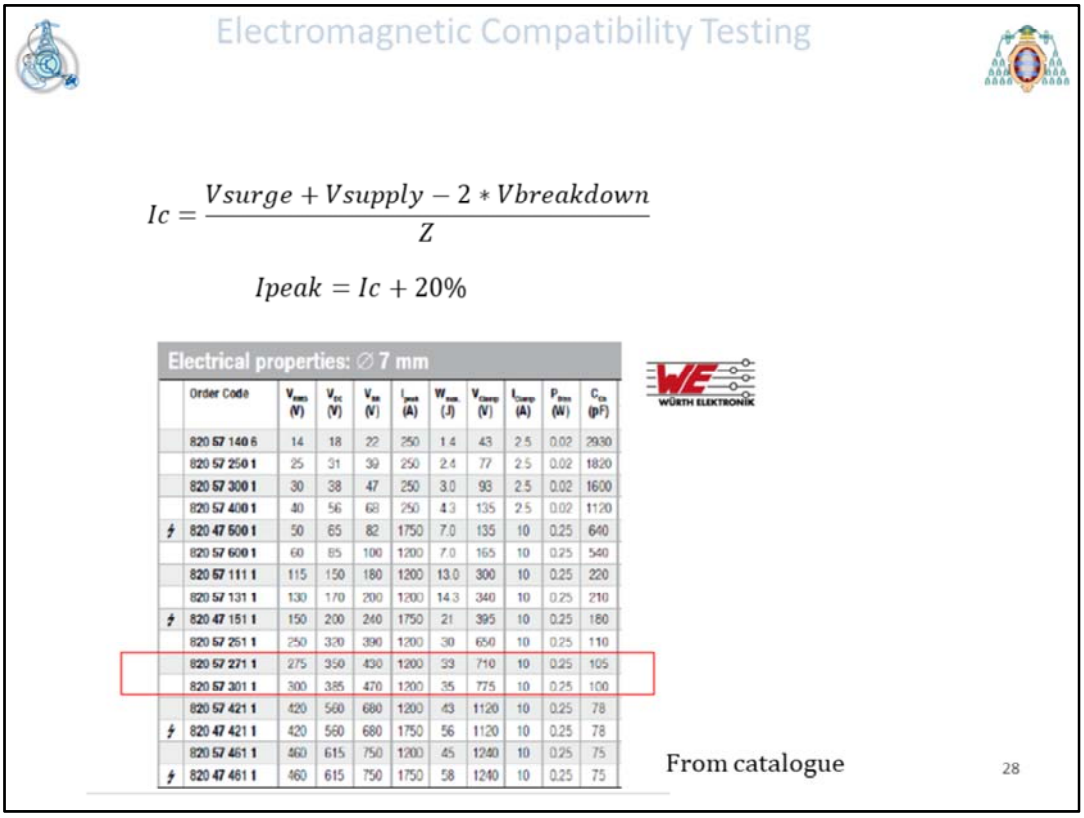
Both circuits in the figure try to reduce common-mode currents by including an EMI filter, but in the circuit of the left the dispersion inductance of the filter deteriorates the operation of the converter, causing overvoltages across the switch.



The figures show the placement of voltage suppressors and how they act in case of an 8-kV overvoltage

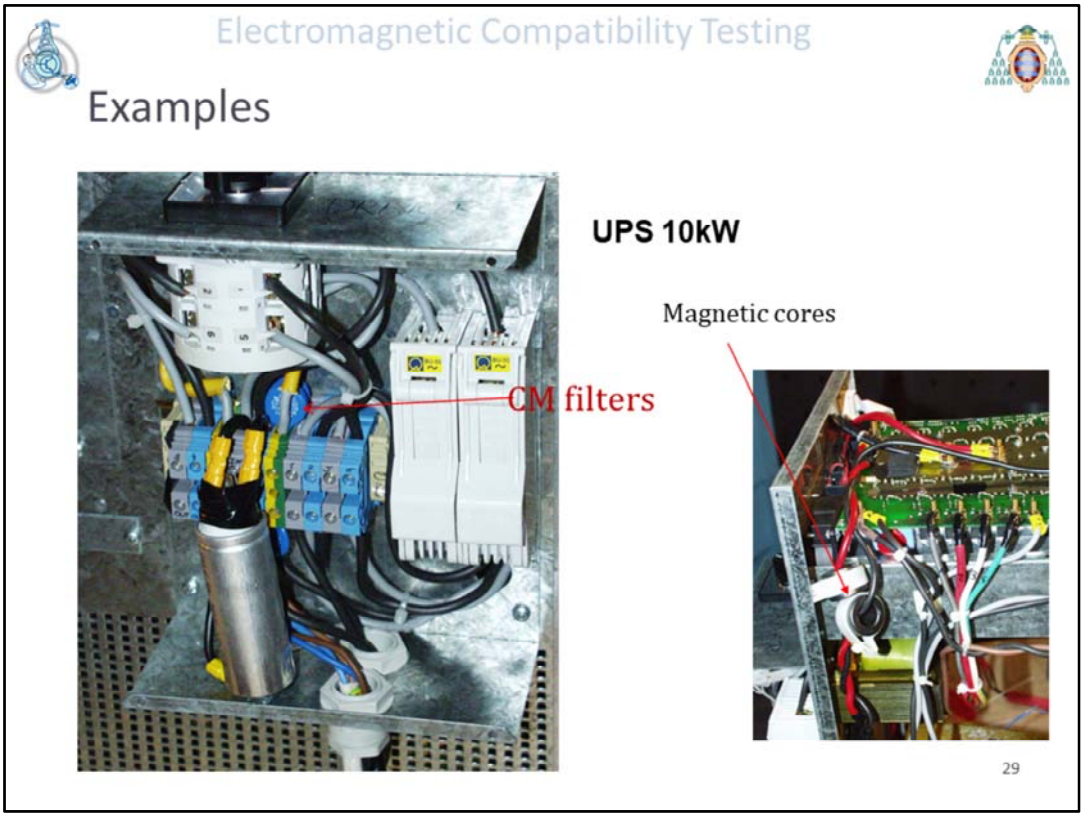


The presence of a varistor implies the circulation of normally negligible leakage currents. When the overvoltage appears, the varistor will have to support the energy that has not reached the circuit to avoid its deterioration.



	Order Code	V_{rms} (V)	V_{dc} (V)	V_{cl} (V)	I_{peak} (A)	W_{max} (J)	V_{clamp} (V)	I_{clamp} (A)	P_{max} (W)	C_{typ} (pF)
	820 57 140 6	14	18	22	250	1.4	43	2.5	0.02	2930
	820 57 250 1	25	31	39	250	2.4	77	2.5	0.02	1820
	820 57 300 1	30	38	47	250	3.0	93	2.5	0.02	1600
	820 57 400 1	40	56	68	250	4.3	135	2.5	0.02	1120
ϟ	820 47 500 1	50	65	82	1750	7.0	135	10	0.25	640
	820 57 600 1	60	85	100	1200	7.0	165	10	0.25	540
	820 57 111 1	115	150	180	1200	13.0	300	10	0.25	220
	820 57 131 1	130	170	200	1200	14.3	340	10	0.25	210
ϟ	820 47 151 1	150	200	240	1750	21	395	10	0.25	180
	820 57 251 1	250	320	390	1200	30	650	10	0.25	110
	820 57 271 1	275	350	430	1200	33	710	10	0.25	105
	820 57 301 1	300	385	470	1200	35	775	10	0.25	100
	820 57 421 1	420	560	680	1200	43	1120	10	0.25	78
ϟ	820 47 421 1	420	560	680	1750	56	1120	10	0.25	78
	820 57 461 1	460	615	750	1200	45	1240	10	0.25	75
ϟ	820 47 461 1	460	615	750	1750	58	1240	10	0.25	75

The selection of the suppressor is made based on the maximum voltage to be allowed and the current that can circulate through the device.



You can visualize the position of filter capacitors in the power input

PCB design

Emissions sources:

- Oscillators , quartz crystal (Harmonics + fundamental frequency)
- High di/dt – dv/dt circuits
- Amplifiers
- Power supplies

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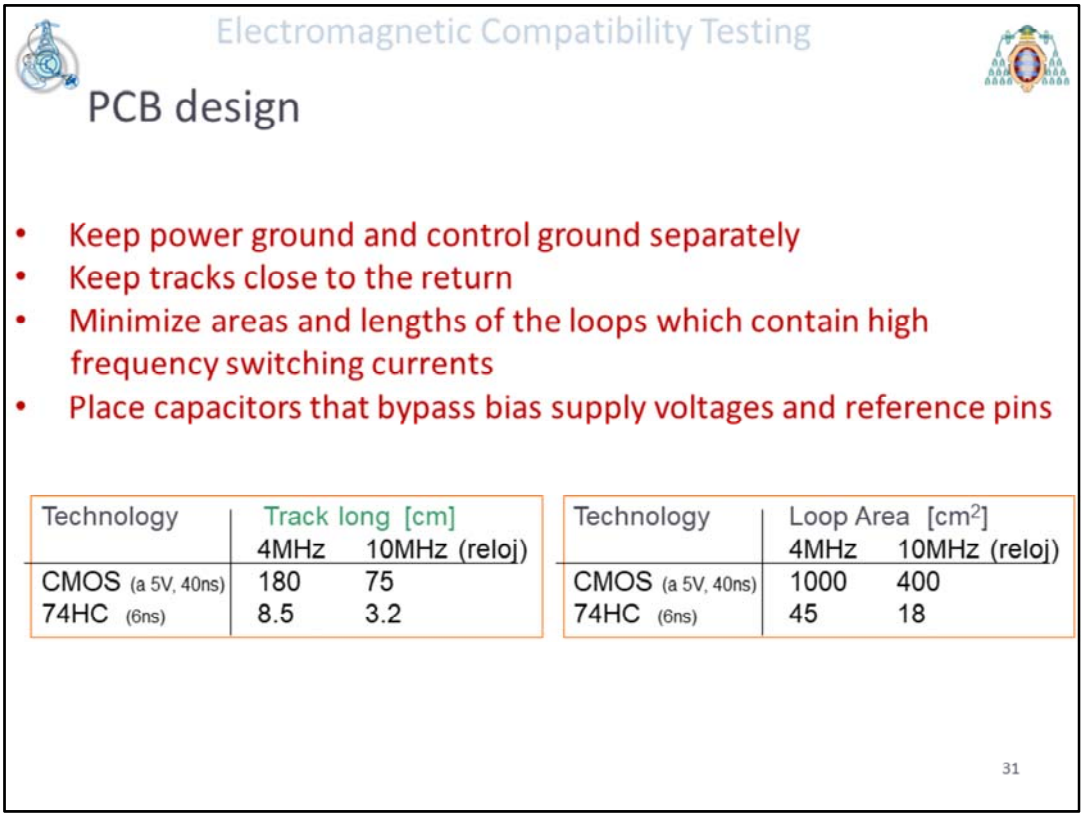
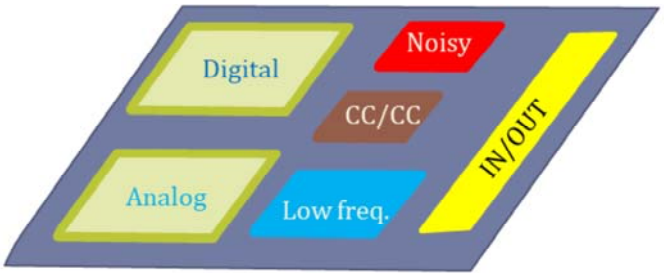


Basic PCB design rules

PCB design

- Power traces drawn first
- Signal traces kept short
- Power ground (good solution)
- Do not mix different type of circuits (Digital, power, RF…)



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PCB design

- These are your critical traces—Route them 1st!
- The 3:1 length:width Rule
- Use planes and copper pours when possible
- 2-layer vs. 4-layer PCBs

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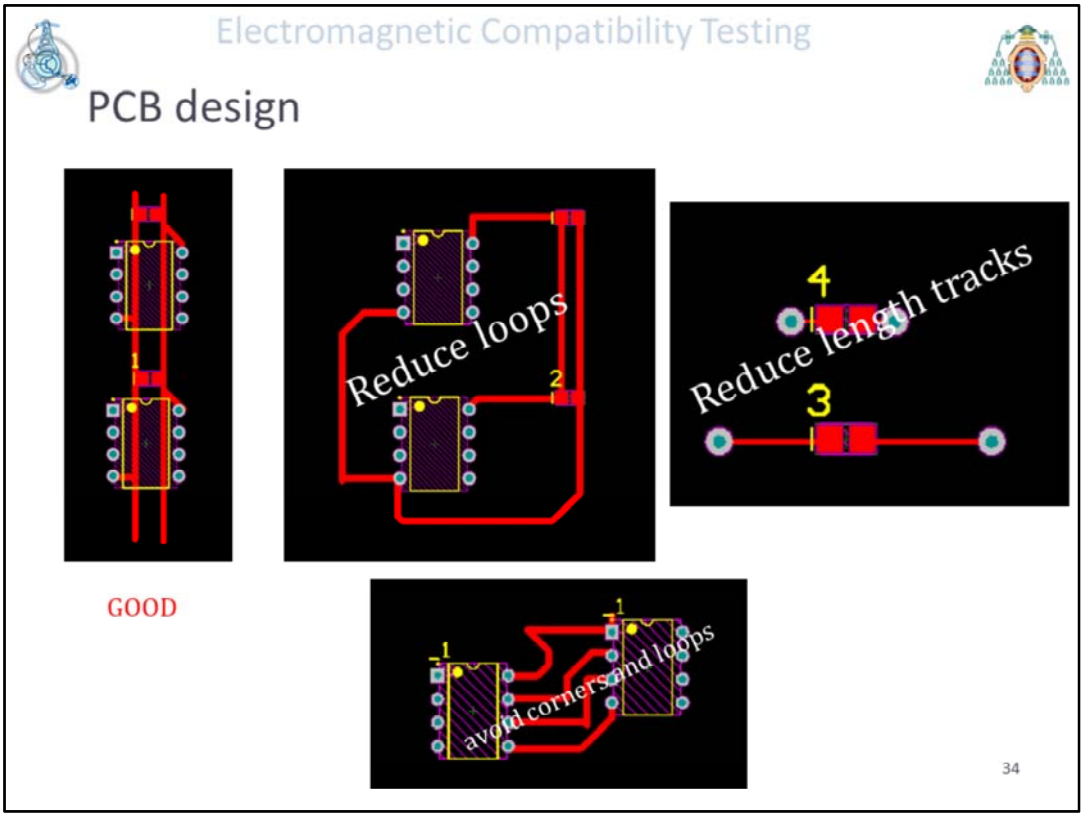
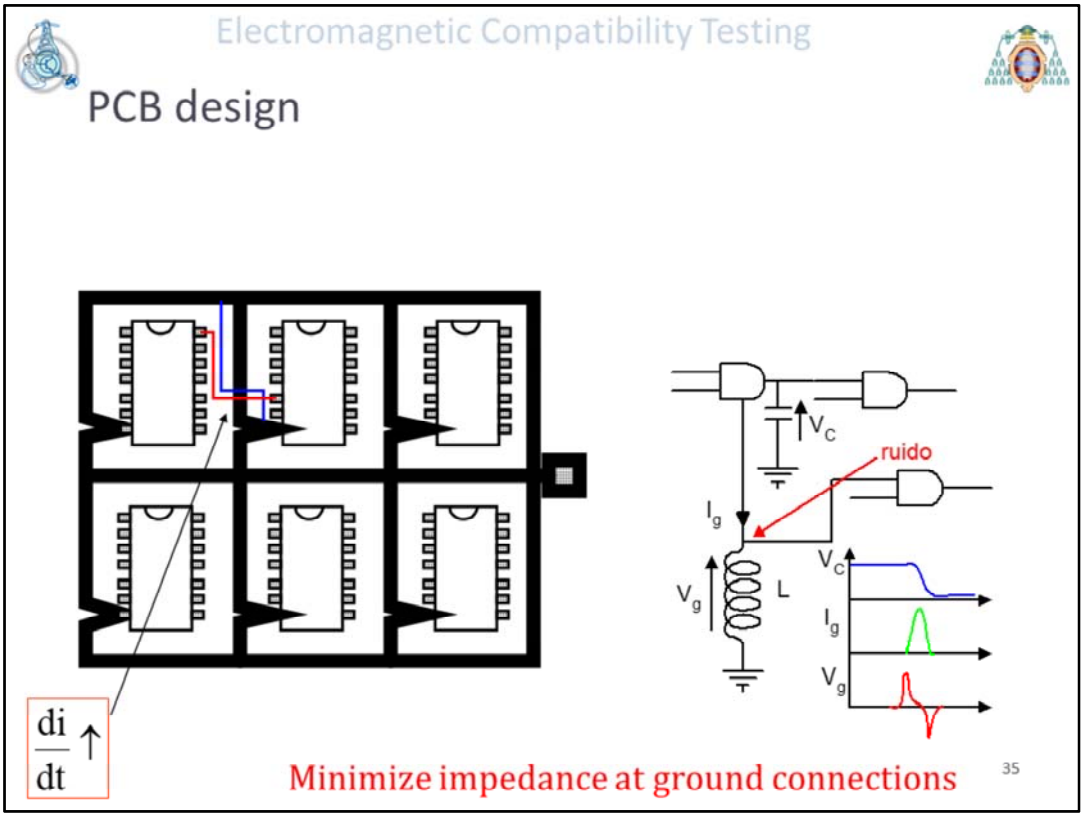
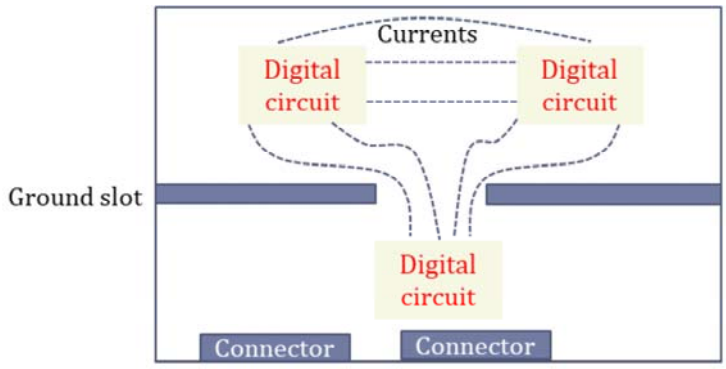


Examples of incorrect track paths on a PCB are shown, and the correct path with the decoupling capacitors as close as possible to the integrated circuit



Reducing the loops that form the tracks is a critical aspect. When a noisy track is identified, adding a return track as close as possible reduces noise emission and improves susceptibility behavior. The figure on the right shows how an unexpected signal can be produced in one of the inputs of the AND gate if the ground connection is made with a high impedance.

Isolated Analog Section Using Cut in Ground Plane to Improve Performance



A well-placed gap in the ground plane can protect circuits located in a particular region of the board from low-frequency return currents flowing in the plane

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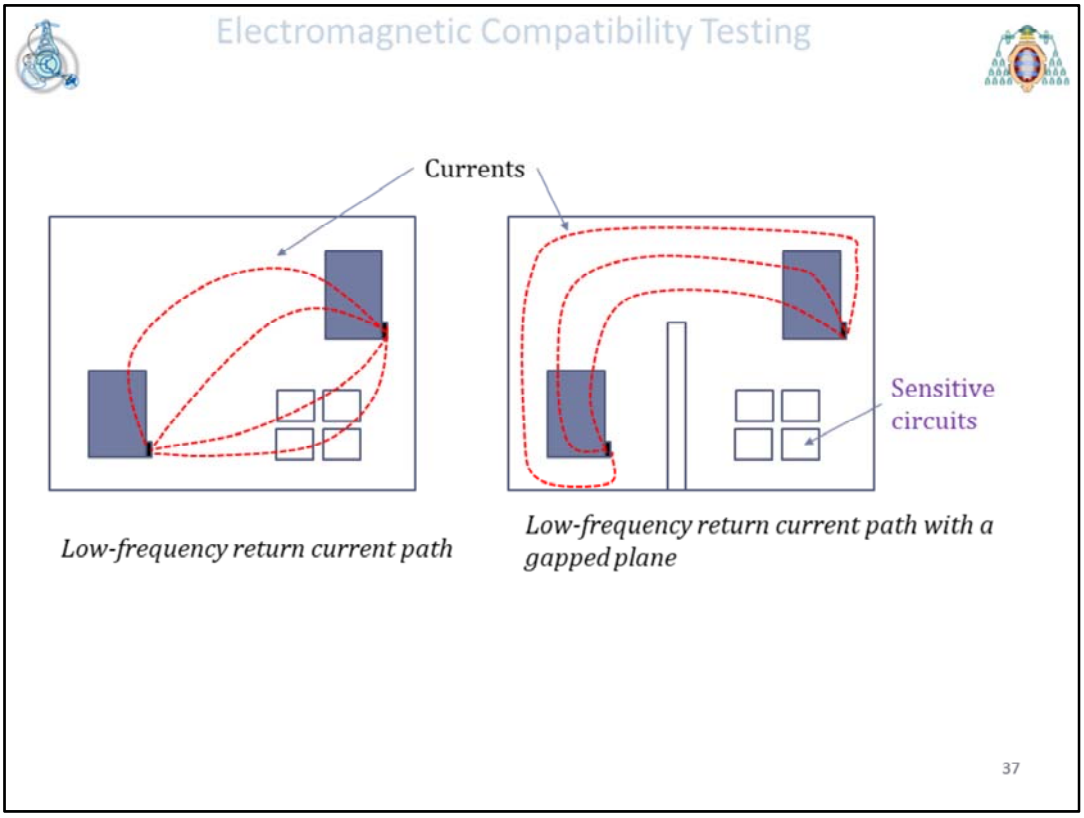
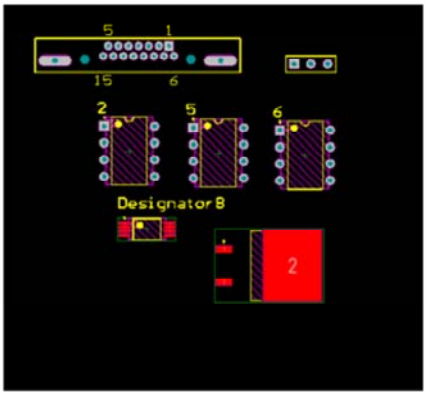
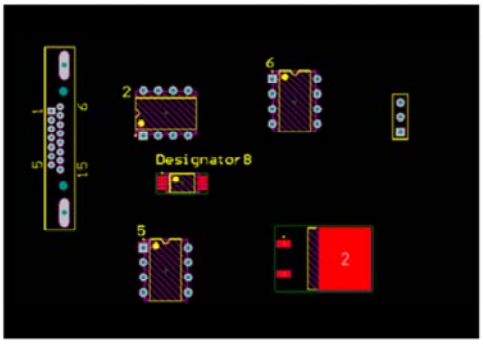
The incorporation of cuts in the ground plane allows to condition the circulation of current in certain areas



When sensitive circuits are affected by the returns of noisy currents, cuts in the ground plane can isolate these circuits avoiding that they are affected by the noisy currents





Bad positioning

Most printed circuit operate at near field when frequencies are below 100 MHz ($\lambda > 3$ meters). This implies that any efficient antenna parts must be relatively large compared to most of the board components. The connectors and chassis connections represent possible efficient antenna parts. By reducing distances, the effect of possible antennas is reduced.

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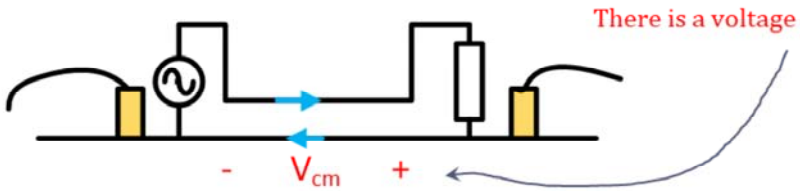

When two connectors are located next to each other, it is unlikely that magnetic fields will induce enough voltage between them to cause a problem

While it is true that the voltages induced across the plane are generally a few orders of magnitude lower than the signal voltages, a few millivolts of noise on an efficient antenna is sufficient to exceed FCC and CISPR radiated emissions requirements

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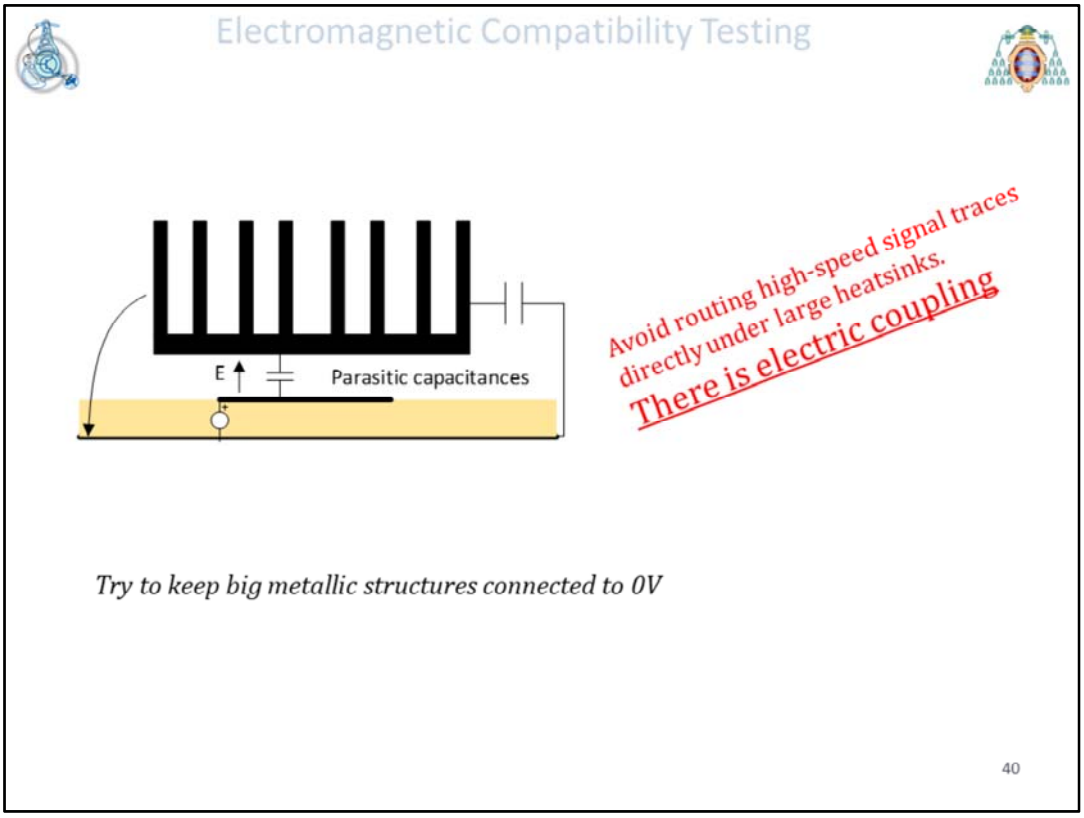
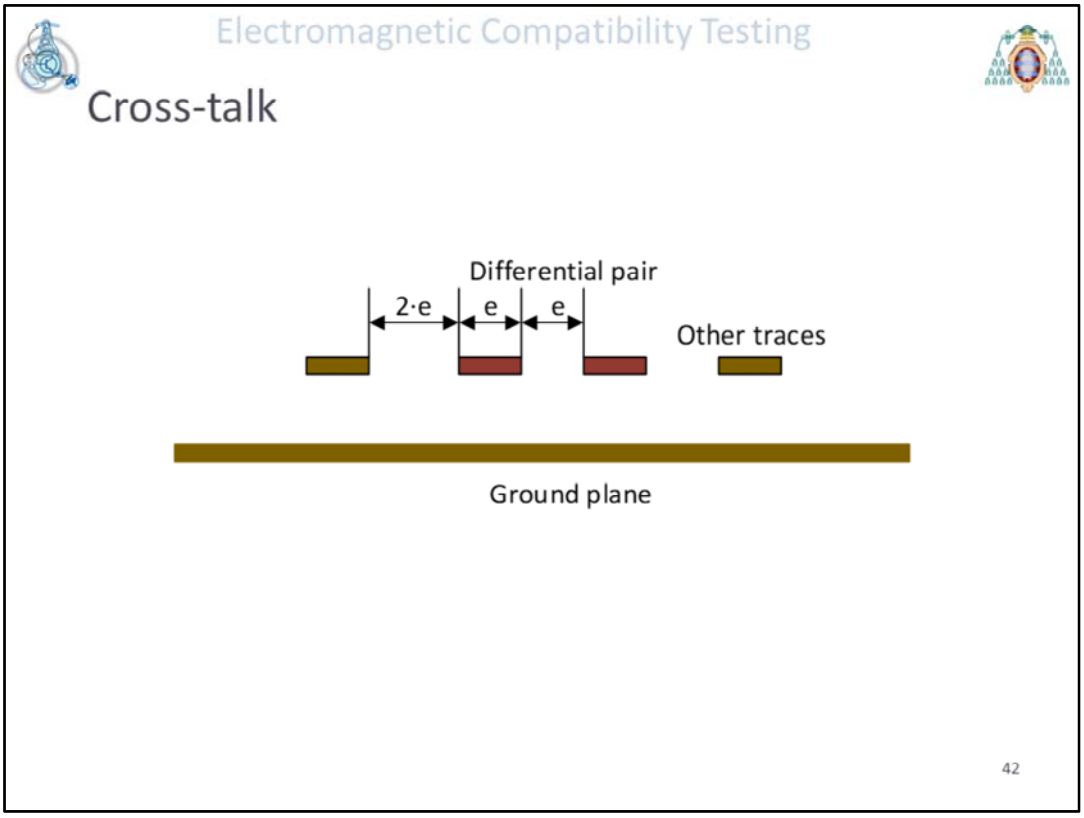
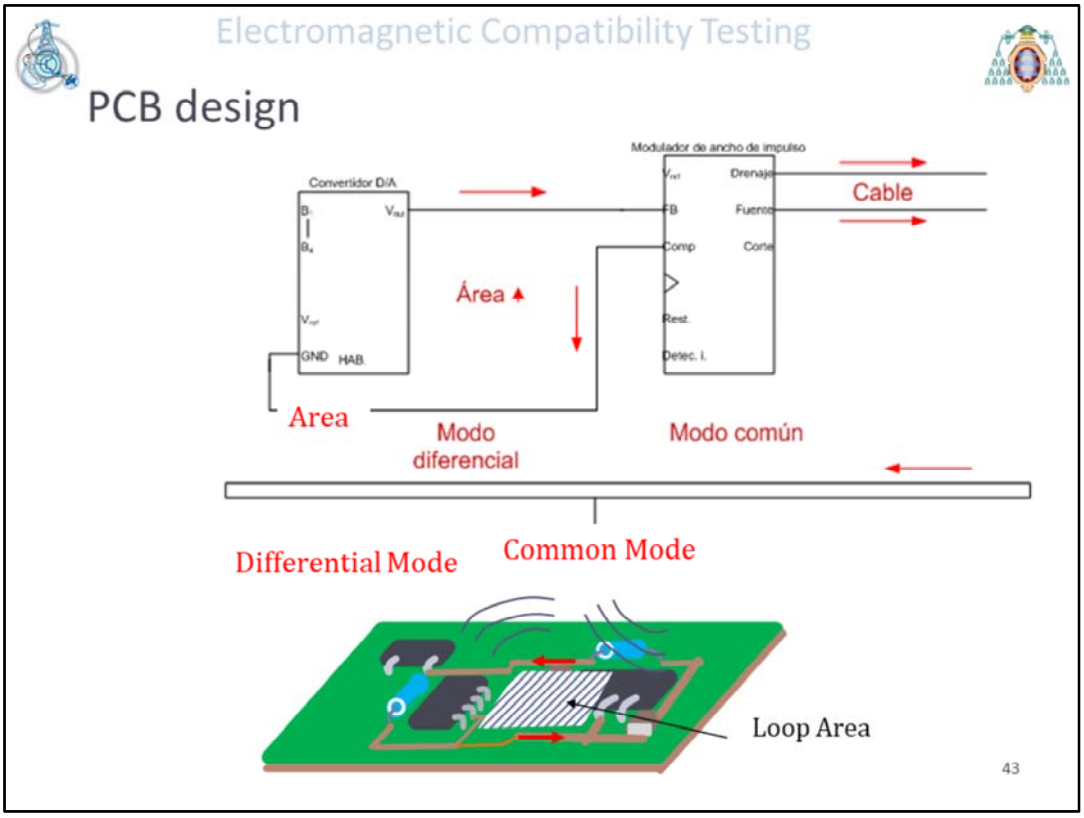


Metal structures such as heatsinks have parasitic abilities with the rest of the circuit. These parasitic capabilities can lead to low-impedance paths for common-mode currents

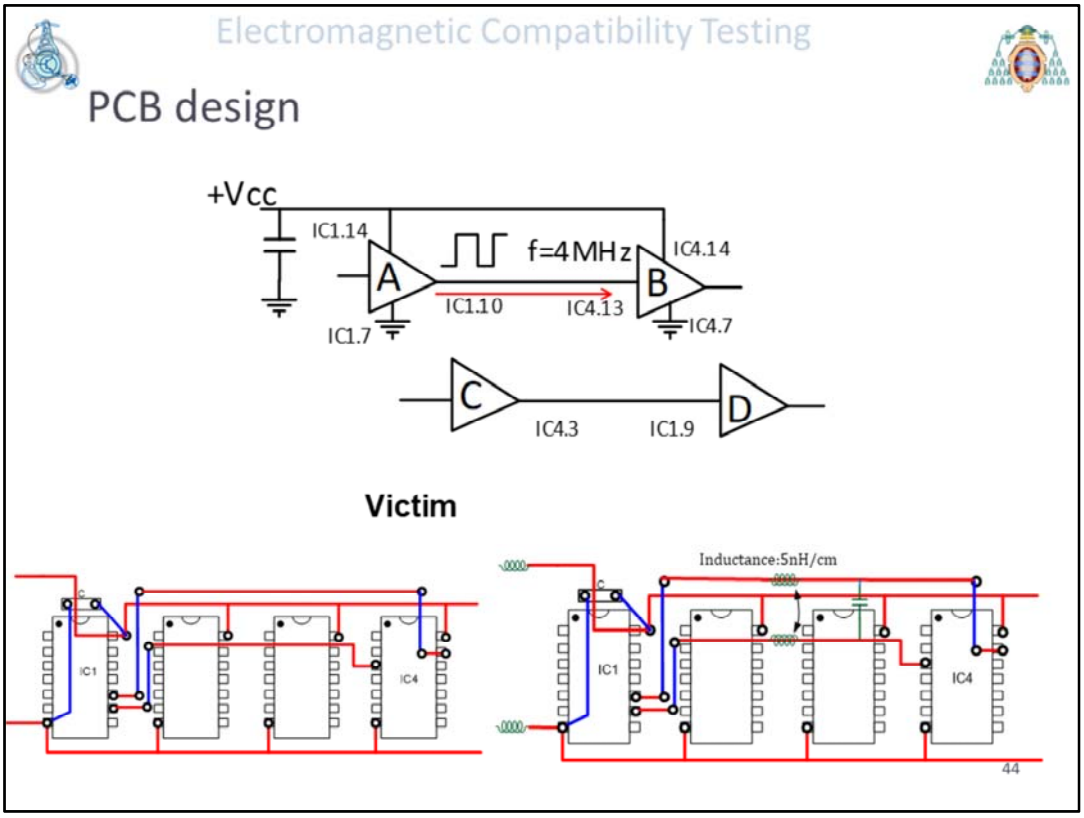
Good antenna	
<100MHz	>100MHz
cables	heatsink
	Power planes
	High components
	Openings in the shield



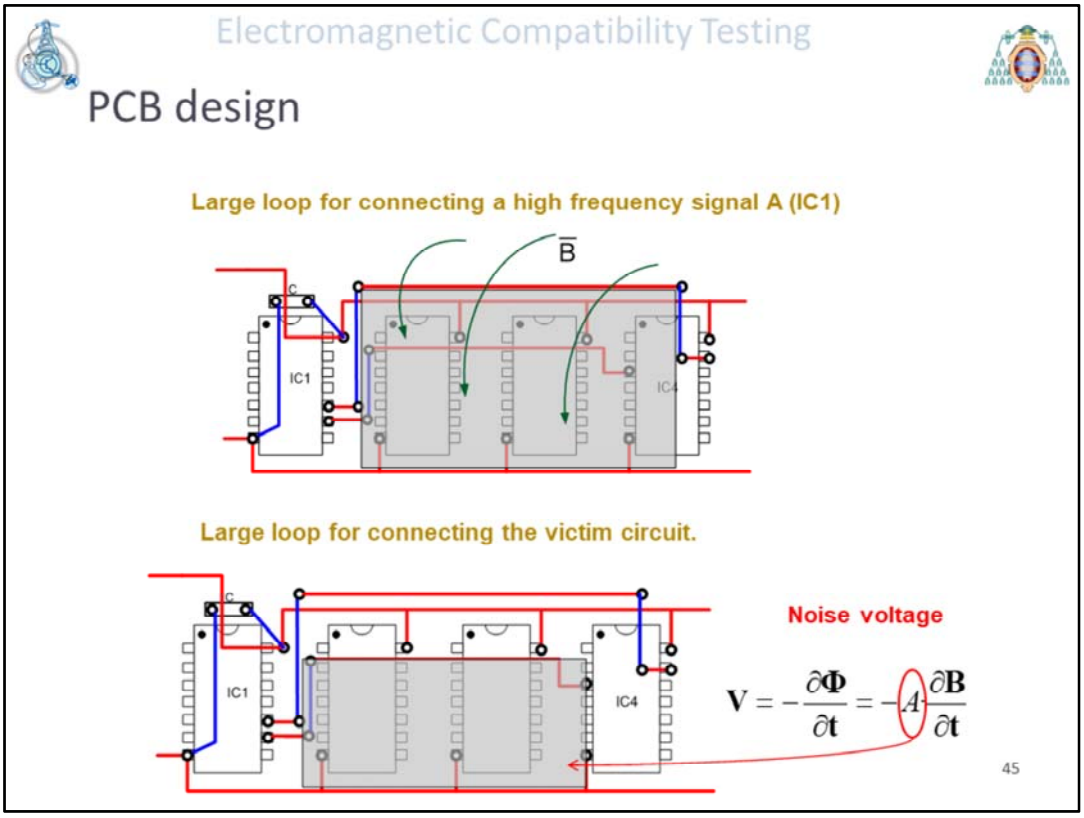
A rule of thumb to reduce cross-talk is making the distance between tracks must be at least twice their thickness



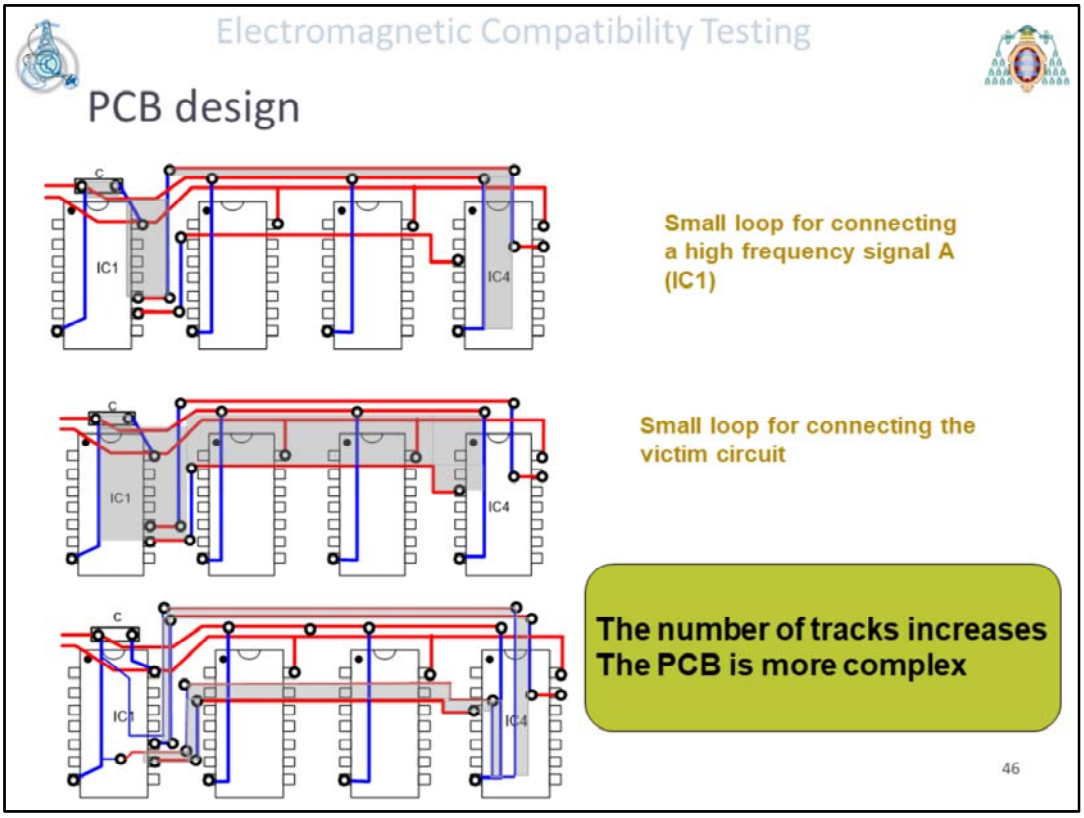
Large areas cause electromagnetic radiation and make the circuit less immune to outside radiation, since noise voltages induced are proportional to magnetic flux variation



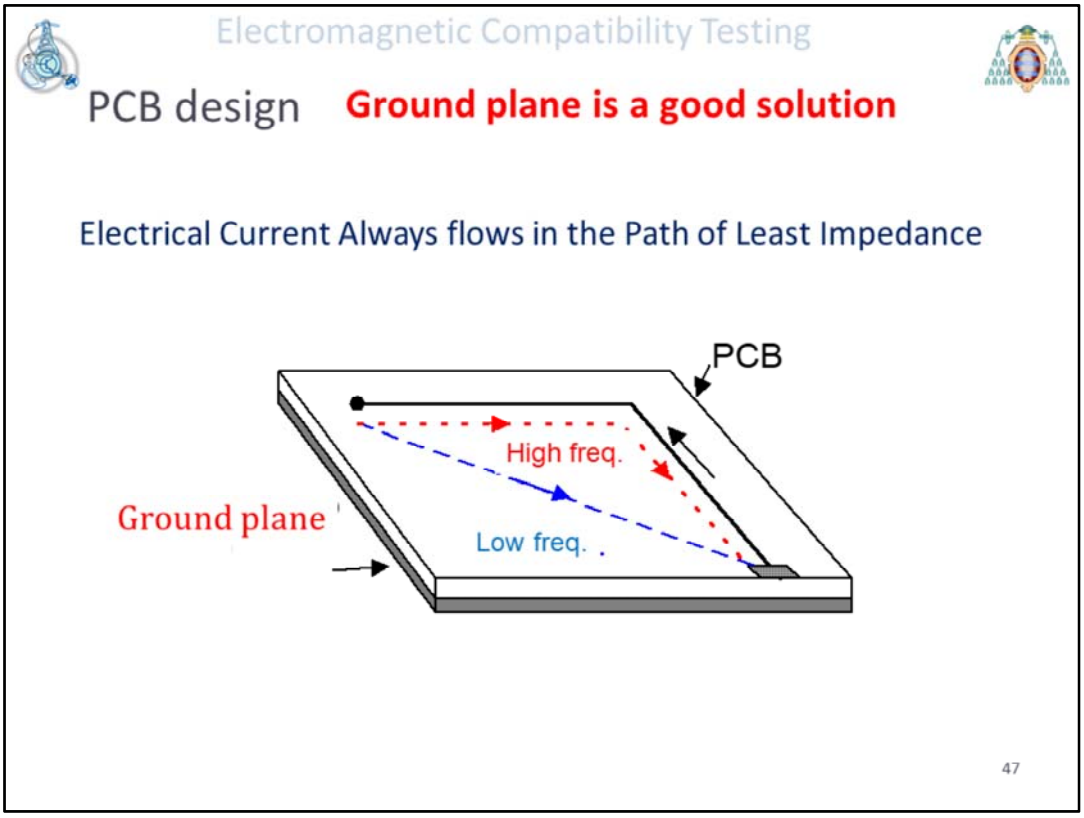
Let's see how we can improve the interconnection of the circuits shown. Although the layout of the tracks is correct, the elements present in the circuit can deteriorate their operation



The presence of large areas reduces the immunity of the circuit. Therefore, a basic design rule that must always be kept in mind is to minimize the area of loops

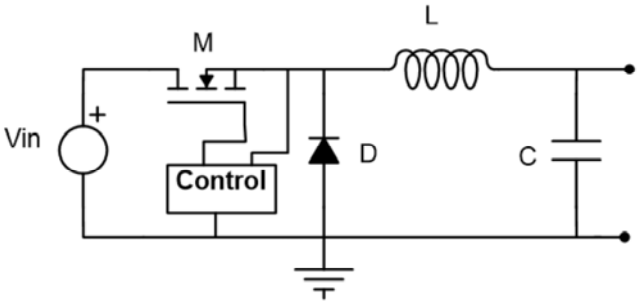


The final design implies a greater number of tracks and greater complexity in the design

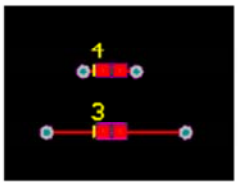


In high frequency, the path of least impedance is the one that minimizes parasitic inductance, i.e. the return path that defines a smaller area. On the contrary, at low frequency the parasitic inductance is negligible and therefore the lowest impedance is achieved with the shortest path

PCB design



Connections with lower inductance will be more effective at higher frequencies.



0.5nH

5nH

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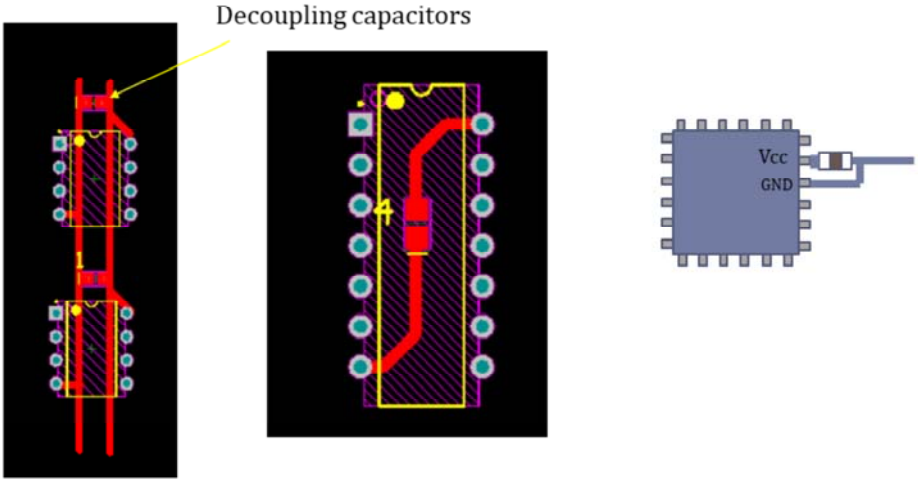
PCB design



Good local decoupling capacitor connections to boards without power planes

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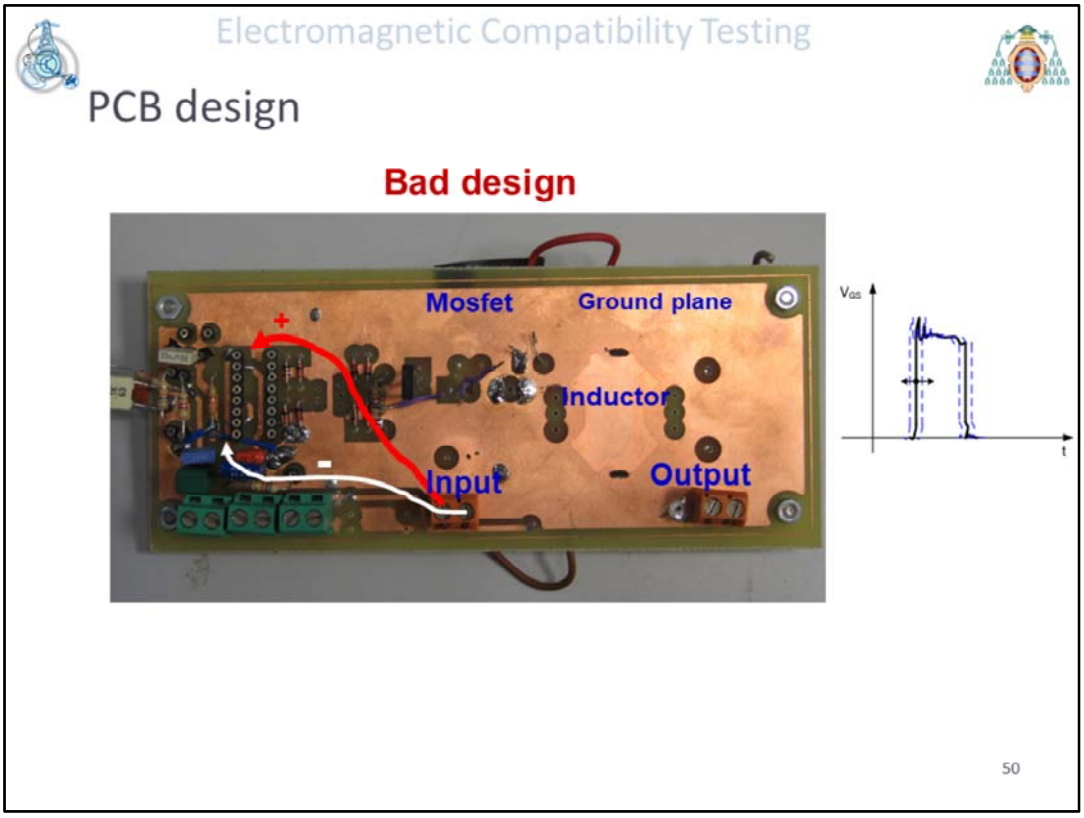
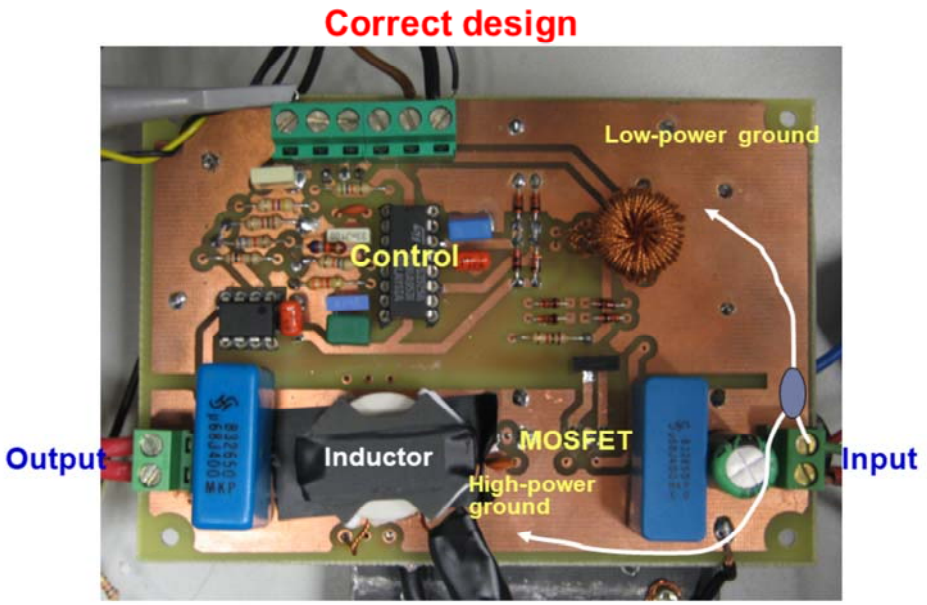


The noise generated by the power currents affect the control circuitry

PCB design



The separation of the ground planes and their connection in a single point corrects the malfunctioning shown in the previous slide

Printed Circuit Board Design Guidelines

1. The lengths of traces carrying high-speed digital signals or clocks should be minimized.
High-speed digital signals and clocks are often the strongest noise sources. The longer these traces are, the more opportunities there will be to couple energy away from these traces. Remember also, that loop area is generally more important than trace length. Make sure that there is a good high-frequency current return path very near each trace.
2. The lengths of traces attached directly to connectors (I/O traces) should be minimized.
Traces attached directly to connectors are likely paths for energy to be coupled on or off the board.
3. Signals with high-frequency content should not be routed beneath components used for board I/O.
Traces routed under a component can capacitively or inductively couple energy to that component.
4. All connectors should be located on one edge or on one corner of a board.
Connectors represent the most efficient antenna parts in most designs. Locating them on the same edge of the board makes it much easier to control the common-mode voltage that may drive one connector relative to another.
5. No high-speed circuitry should be located between I/O connectors.

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Printed Circuit Board Design Guidelines

6. Critical signal or clock traces should be buried between power/ground planes.
Routing a trace on a layer between two solid planes does an excellent job of containing the fields from these traces and prevents unwanted coupling.

7. Select active digital components that have maximum acceptable off-chip transition times.
If the transition times of a digital waveform are faster than they need to be, the power in the upper harmonics can be much higher than necessary. If the transitions times of the logic employed are faster than they need to be, they can usually be slowed using series resistors or ferrites.

8. All off-board communication from a single device should be routed through the same connector.
Many components (especially large VLSI devices) generate a significant amount of common-mode noise between different I/O pins. If one of these devices is connected to more than one connector, this common-mode noise will potentially drive a good antenna. (The device will also be more susceptible to radiated noise brought in on this antenna.)

9. High-speed (or susceptible) traces should be routed at least 2X from the board edge, where X is the distance between the trace and its return current path.
The electric and magnetic field lines associated with traces very near the edge of a board are less well contained. Crosstalk and coupling to and from antennas tends to be greater from these traces.

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Printed Circuit Board Design Guidelines

10. Differential signal trace pairs should be routed together and maintain the same distance from any solid planes.

Differential signals are less susceptible to noise and less likely to generate radiated emissions if they are balanced (i.e. they have the same length and maintain the same impedance relative to other conductors).

11. All power (e.g. voltage) planes that are referenced to the same power return (e.g. ground) plane, should be routed on the same layer.

If, for example, a board employs three voltages (say 3.3 volts, 3.3 volts analog and 1.0 volt), then it is generally desirable to minimize the high-frequency coupling between these planes. Putting the voltage planes on the same layer will ensure that there is no overlap. It will also help to promote an efficient layout, since the active devices are unlikely to require two different voltages at any one position on the board.

12. The separation between any two power planes on a given layer should be at least 3 mm.

If two planes get too close to each other on the same layer, significant high-frequency coupling may occur. Under adverse conditions, arcing or shorts may also be a problem if the planes are too closely spaced.

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Printed Circuit Board Design Guidelines

13. On a board with power and ground planes, no traces should be used to connect to power or ground. Connections should be made using a via adjacent to the power or ground pad of the component.

Traces on a connection to a plane located on a different layer take up space and add inductance to the connection. If high-frequency impedance is an issue (as it is with power bus decoupling connections), this inductance can significantly degrade the performance of the connection.

14. If the design has more than one ground plane layer, then any connection to ground at a given position should be made to all of the ground layers at that position.

The overall guiding principle here is that high-frequency currents will take the most beneficial (lowest inductance) path if allowed to. Don't try to direct the flow of these currents by only connecting to specific planes.

15. There should be no gaps or slots in the ground plane.

It's usually best to have a solid ground (signal return) plane and a layer devoted to this plane. Any additional power or signal current returns that must be DC isolated from the ground plane should be routed on layers other than the layer devoted to the ground plane.

16. All power or ground conductors on the board that make contact with (or couple to) the chassis, cables or other good "antenna parts" should be bonded together at high frequencies.

Unanticipated voltages between different conductors both nominally called "ground" are a primary source of radiated emission and susceptibility problems.

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Printed Circuit Board Design Guidelines

17 it's a good idea to put the components that send or receive signals through the connector nearest the connector (<2cm).

18 Components not connected to an I/O net should be located at least 2 cm away from I/O nets and connectors.

19 Power planes on the same layer must have at least a 3-mm gap between them. Critical nets should be routed at least 2X from the board edge, where X is the distance between the trace and its return current path.

Common sources of EMI problems include

- Power Supply Filters
- Ground Impedance
- Inadequate Signal Returns
- LCD Emissions
- Component Parasitics
- Poor Cable Shielding
- Switching Power Supplies (DC/DC Converters)
- Internal Coupling Issues
- ESD In Metalized Enclosures
- Discontinuous Return Paths

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